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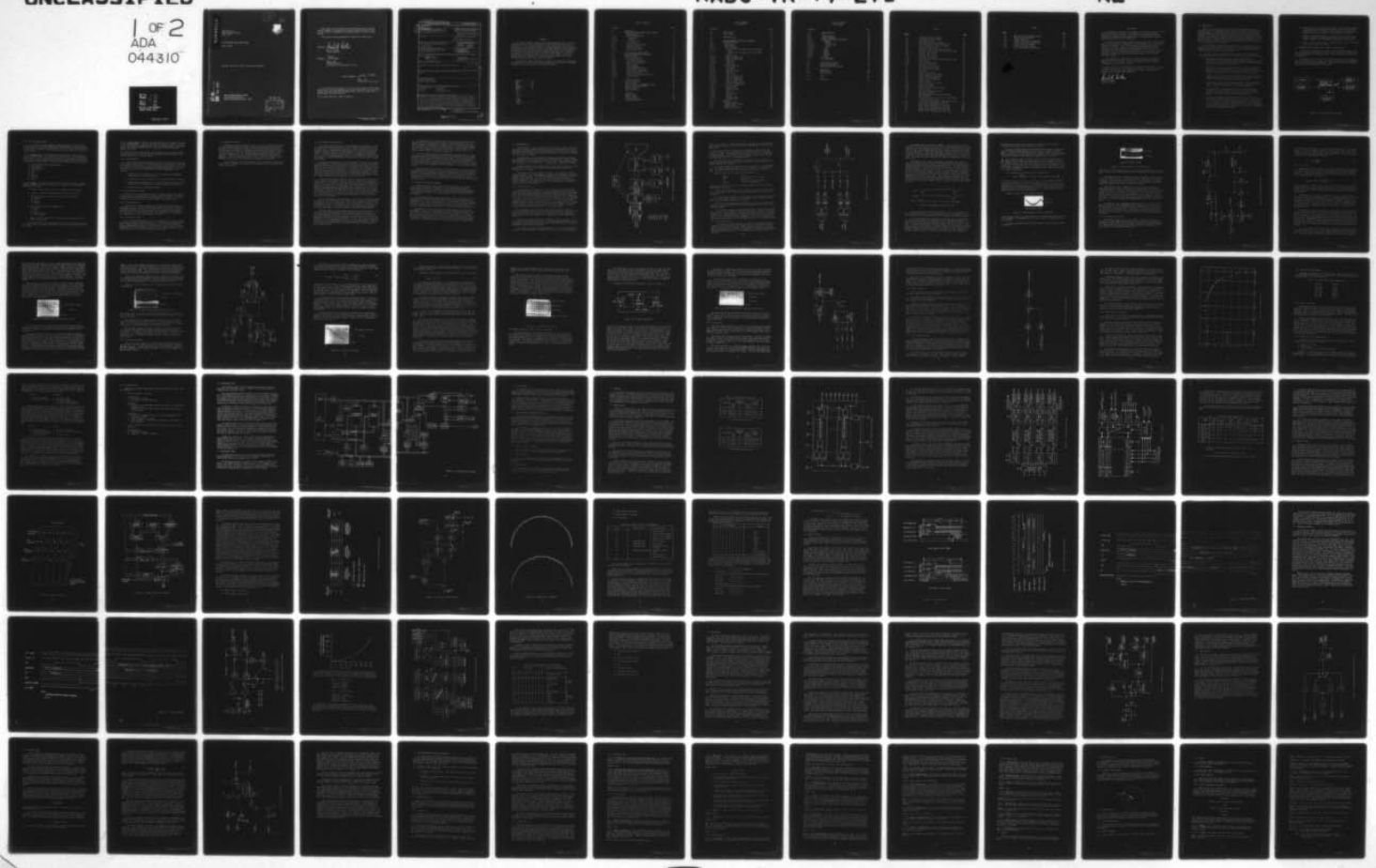

RADC-TR-77-271
Final Technical Report
August 1977

COLOR TERMINAL DEVELOPMENT STUDY

Sperry Univac

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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A feasibility effort was conducted to determine the difficulties inherent in enhancing an existing dual-screen display terminal with color cathode ray tubes. Two high resolution color CRTs were acquired. Necessary monitor circuitry was modified from the original or developed, including a digital convergence concept. A mock-up (brassboard) was built and demonstration at a 525 TV line standard with text and graphics demonstration software. An Advent color projector was modified to accept high bandwidth color signals from the demonstration terminal.

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SUMMARY

The greatly increased capability of electronic communication systems has created a pressing need for expanded data output capacity in all fields of application. In the information analysis and interpretation field there is a particular need for enhanced techniques for visual presentation and, especially, for methods of increasing the amount of information which can be effectively communicated to the receiver using a standard visual image. The introduction of color to digital CRT display screens offers a direct method of further multiplying the information capacity of these visual images. Color offers added potential for emphasis of critical message content, more attractive message presentation, and reduced operator fatigue.

This technical report addresses the results of a study made to determine the feasibility of a direct view color terminal and the technical achievements required to incorporate color in terminal applications.

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EVALUATION

As a beginning point this study assumed the existence of the dual screen Sperry-Univac 1652 or OJ-389(V). The question to be studied was the feasibility of adding color to the OJ-389(V). This study addressed the technological approaches and problems that are introduced into a computer terminal design when color is considered.

An obvious central technical problem was the selection of an appropriate color CRT with sufficient resolution in a small enough size to fit physical terminal requirements. Such a high resolution tube was found in both a 15 inch and 13 inch size. They are of shadow mask design and whereas a conventional 15 inch color CRT contains 290,000 dot trios, the high resolution tube has 910,000 dot trios deposited on the CRT face. Images of excellent quality were obtained from these tubes in 6 colors plus black and white of 2000 character arrays and dense graphics on a 640 x 480 addressable matrix.

The combination of high resolution, small color CRTs, available 4K RAM memories for image memory and an effective microcomputer produced a highly useful color terminal. Subjective reactions to the brassboard demonstration unit were very positive.

Equally positive was the reaction to large screen projections of color terminal presentations on an Advent color projector. The Advant, normally an off-air TV projector, was stripped of its receiver front-end and presented with separate 17MHz RGB inputs.

David A. Luther

DAVID A. LUTHER
Project Engineer

1.0 INTRODUCTION

This technical report is a result of a color enhancement study conducted for Rome Air Development Center (RADC) by the Defense System Division of Sperry Univac, St. Paul, Minnesota. The overall objective of this study was to determine the feasibility of adding color to direct viewing terminal displays. This study also addressed the technological approaches and problems that are introduced into a terminal design when color is considered. To support this study, a working non-deliverable demonstration "breadboard" color display model was constructed to verify study findings and allow demonstrations of color capability to the customer.

Areas of design and characteristics unique to the color study are described in detail in the text of this report, while areas similar to the operations of the OJ-389(V) Dual Display Unit, i.e., the central processor and associated logic, are covered more generally.

Specific objectives established for the study are identified in the following subparagraphs and are discussed in detail in the test of this report:

a. Demonstration/Development Model, General Characteristics - Discussion is directed toward the supply and/or procurement of color monitors for possible production use. Coverage includes convergence characteristics of high resolution CRTs.

b. Controller - Discussion is centered around the logical structure of the controller area designed into the color demonstration unit. Because of its similarity to the OJ-389(V), discussion is limited to general characteristics and differences between the two units.

c. Graphics - Discussion is directed to memory trade-offs and the resulting design incorporated in the demonstration model. Organization of the design and control are explained in detail.

d. Video Inputs - Discussion is directed to input composite video signals for display on the screen as an overview. Consideration is given to various chroma circuit ICs and video amplifiers.

e. Video Amplifier - The characteristics of a video amplifier are identified. The requirements of this phase of design are made unique by the need to control saturation levels and prevent the mixing of the overlay video signal and digital inputs.

f. Interface Requirements - Since the demonstration unit was not equipped with an I/O interface circuit, discussions in this section are limited. The basic requirements for various I/O configurations is not considered a technical breakthrough for a color terminal; rather color bit assignments are made in the format of 1652 graphics to indicate minimum impact to host computer software when addressing both color and monochrome terminals.

g. Software Structure and Operating Procedures - This section addresses the structure of the software as designed for the color terminal demonstration unit. Discussion is also directed to operating procedures based on the structure of both hardware and software.

h. Packaging - Proposed packaging concepts for both dual and single monitor terminals are shown and discussed in this section of the report. Both 13 and 15 inch CRTs are depicted in this section.

i. Summary - This section contains a summary of the results of the study that is the basis of this report.

1.1 DEMONSTRATION/DEVELOPMENT MODEL, GENERAL CHARACTERISTICS

To support and compliment this study, a non-deliverable breadboard device was constructed. This device incorporated pertinent features of a color unit although functional capability rather than final design for production was emphasized.

As required by the study contract, a demonstration of the development model was held in St. Paul. Figure 1.1 shows the configuration of equipments used in the demonstration presentation. Characteristics of these equipments are described in the following subparagraphs.

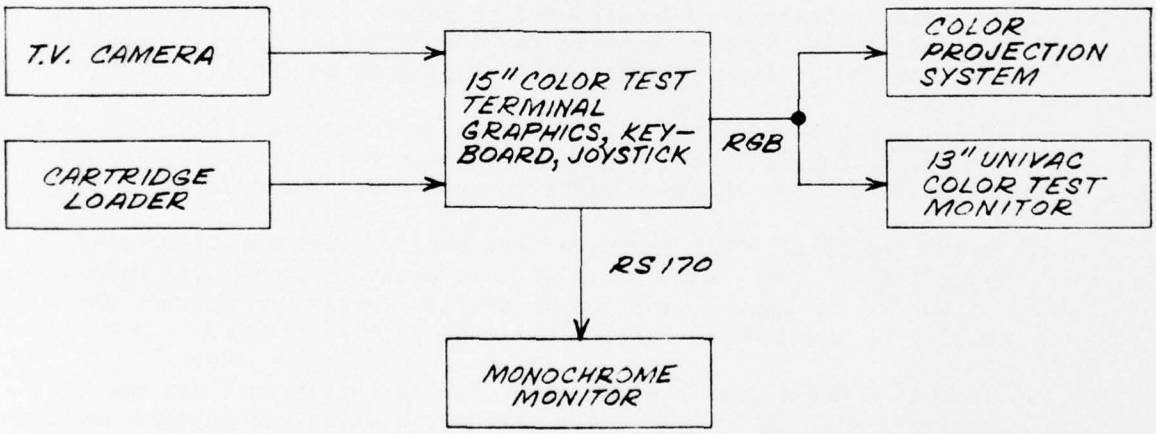


Figure 1.1 Demonstration Block Diagram

1.1.1 The Development Model

The 15 inch color test terminal or development model consisted of the hardware necessary to perform alphanumeric presentations in seven selectable colors; enhanced graphics with the capabilities of displaying circles, vectors, vector strings, and arcs in some selectable colors; and composite video overlays in color.

1.1.1.1 Alphanumerics - The alphanumeric presentation was demonstrated in seven selectable colors: red, green, blue, yellow, white, cyan, and magenta. Other features controlled by keyboard operation included reverse video, where a black character was inserted on one of the seven color fields; blinking; and protection of character fields. Editing of the alphanumeric screen included:

a. Cursor movement keys including HOME
b. Line delete
c. Character delete
d. Word delete
e. Move
f. Copy
g. Rub out
h. New Line
i. Insert
j. Protect

1.1.1.2 Graphics- The graphics section of the terminal consisted of enhanced graphics capability as well as interactive or operator-controlled graphics. Capabilities included:

a. Graphic cursor active - places a red cross hair on the screen.

b. Joystick - controls the movement of the cross hair cursor.

c. Function switches - control the function to be performed:
   1) Generate
   2) Erase
   3) Blink
   4) Restore

d. Type switches - select the graphic type:
   1) Vector
   2) Circle
   3) Arc
   4) Vector string
   5) End of string

e. Mark - Enters a coordinate for a given type and function in to the terminal controller.

A detailed description of the keyboard and interactive operator functions are found in Section 7 of this report and are therefore omitted in this section of the text.

1.1.1.3 Color Cluster - Unique to the color terminal is the addition of eight color cluster switches. With these switches the operator can select the color of the presentation being added to the screen in both alphanumeric and graphic modes. The selectable colors include: red, blue, green, yellow, cyan, magenta, and white.

The eighth switch is labeled as SAT. In the graphic mode, this switch allows the operator to color in or tint circles and enclosed vector strings in the desired saturation of a selected color.

1.1.2 13 Inch Monitor

As part of the study, and in support of monitor procurement requirements, Sperry Univac designed and built a high resolution, 13 inch monitor. This unit was equipped with receivers for R, G, and B data, and video amplifiers to allow the receipt of video data transmitted from the demonstration model. The construction of this unit then satisfies the following requirements of the contract:

a. Demonstrates the capability to receive and display retransmitted screen data on an external monitor.

b. Provides for a source of monitors for possible production follow-ons.

c. Demonstrates the capability of a 13 inch, high resolution CRT as compared to a 15 inch CRT for use in direct viewing color terminals.

d. Verifies sizing for terminal packaging.

1.1.3 Color Projection System

The use of a color projection system is included to provide the means of demonstrating the color capability to a large number of viewers. The addition of this device also demonstrated the RGB retransmission capability and the ability to project color data on a large screen at an effective cost.

1.1.4 Monochrome Monitor

The monochrome monitor demonstrated the capability for retransmission of screen data in black and white formats using the RS170 technique. In this transmission feature, color data is stripped from the screen data, mixed with sync pulses which are internally generated, and transmitted as a composite video signal over a single coaxial cable. This capability also demonstrates the compatibility of color and monochrome terminals.

1.1.5 Color Camera Inputs

The color camera provides a source for a composite color video to demonstrate color overlays on the display screen. The video data is demodulated via normal chroma techniques used in conventional color TV sets and mixed with digital alphanumerics and graphics for presentation on the screen. Priorities established for this presentation are alphanumerics highest, graphics as the second priority, and finally the composite video picture.

1.1.6 Magnetic Tape Unit

The magnetic tape unit provides a means to load the operational programs into the terminal as well as various static screen presentations that were used during the demonstration program. Microcode programming and associated hardware allow the operator to communicate directly with the magnetic tape unit via the terminal. Two switches are included on the operator's panel to initiate this communication. For initial program loading, the INIT switch is depressed. When initiated, the terminal starts a self-test program and, if successful, loads the operational program into the instruction memory. This self-test and load program is resident in a PROM within the terminal.

The second switch, INIT TAPE, operates from the operational program and allows operator commands to be controlled by screen mode and ID functions displayed on the screen.

2.0 CRT INVESTIGATION AND STUDY

The traditional problem faced in transforming from monochrome to color for digital CRT displays has been the lack of adequate resolution due to the discrete nature of color phosphor deposition currently employed. Color dot densities have been adequate for the display of only about one-third of the number of characters that are readily viewable in an equivalent monochrome screen. A further problem has been that only one phosphor type (P22) has been used for color CRT manufacture, whereas a wide variety of phosphor types are offered for tailoring monochrome CRT screens for specific direct viewing applications.

The beam penetration color CRT was considered for digital color displays by Sperry Univac. In this device, the CRT utilized a multilayer screen comprised of two different color phosphor layers separated by a layer of transparent dielectric material which served as a barrier. The principle of operation was to excite one color phosphor at a voltage of 9 KV, the second at a 16 KV voltage, and the two mixing colors at intermediate voltages. In other words, the accelerating voltage had to be switched from between 9 and 16 KV each time a change in color was required on the display. Furthermore, using this approach restricted the display to, at best, four colors.

Since the accelerating voltage is switched repeatedly in order to make color changes, a proportional correction had to be applied to the magnetic deflection system so that the deflection amplitude was constant regardless of color. At the same time, the beam current had to be modulated to effect constant picture brightness. The advantage of this approach was that the CRT offered a continuous phosphor (as in monochrome displays) instead of the discrete color bar and dot technique offered in the standard CRT. The project was ultimately abandoned as a possible candidate for an alphanumeric display, since the difficulties were too severe and color selectivity too limited. It was concluded that such a display was more applicable to analog type data, such as PPI radar displays.

With the development and introduction of the Trinitron single-gun picture tube into the color CRT market, Sperry Univac again evaluated the possibility of producing a digital color display. This effort produced the capability of displaying 20 lines of 42 characters, each 10 dots wide and 12 dots high, on a 15 inch color tube. By this time, however, most requirements demanded 24 rows of 80 characters on the same size CRT for monochrome compatibility.

Additional CRTs have since become available and were investigated. The 3-in-line gun, segmented phosphor CRT introduced by RCA was examined. The tube design approach was similar to that of the Trinitron and offered the principal advantage; simplified convergence of the beams was the primary disadvantage of the delta-gun, dot-trio type color CRT. This study revealed that the RCA tube offered approximately 640 bars of each color, and the space between one color bar and another of the same color was 0.020 inches. Again it was concluded that CRT could not meet the now-established requirements of 24 rows by 80 characters.

A reexamination of the standard delta gun CRT was initiated after the introduction of the "black matrix" design. It was demonstrated that such a CRT was capable of displaying the required number of characters, but only on a 19 to 25 inch screen While the advantages of color could be demonstrated, the physical size of the display was objectionable to most viewers. Brightness - a basic problem in the earlier tubes - was overcome, and the door started to open toward a feasible color terminal.

In June of 1975, Sperry Univac DSD Engineering became aware of a high resolution color CRT developed by Cathode Ray Tube Division of the Matsushita Electronics Corporation of Takatsuki, Osaka, Japan. The tube had been introduced in Japan in early 1974 and in the United States about the middle of May 1975. Sperry Univac took steps to procure one tube for evaluation. Using a custom-built monitor, a high resolution display of 36 rows of 80 characters in seven colors was accomplished in the laboratory on a 15 inch, direct viewing screen.

The high resolution of this tube is made possible by the increased number of phosphor dots on the screen. A nearly five-fold increase in the number of phosphor dots has been made by reducing the shadow-mask pitch (space between holes) to 0.3 millimeters (0.012 inches), which is less than half that of conventional color picture tubes. A conventional 15 inch color CRT contains 239,000 dot trios, while the high resolution tube has 910,000 dot trios deposited on the CRT face.

2.1 MONITOR SOURCING AND ELECTRONICS

Preceding the award of the study contract and during its execution, Sperry Univac continued to communicate with the Matsushita Electronics Corporation in an effort to establish a specification and packaging concept for a possible production unit. A specification was generated and submitted in support of this effort. Quotes were asked for both 15 inch and 13 inch CRT monitors.

To date, Matsushita has taken exception to the electrical specification in areas of high voltage regulation, focus capabilities, and packaging considerations. They also stated that the 13 inch CRT monitor could not be made available for some time and discouraged its use. As a result of this response, and since monitors would be procured from a single source, Sperry Univac launched a design-and-build effort for a 13 inch, high resolution CRT monitor.

Emphasis was placed on reliability, maintainability, and convergence techniques as well as on a firm design approach. Inquiries were made of the CRT Division of Matsushita Electronics Corporation to establish a source for the CRT. Sperry Univac has been assured of a "smooth supply of the tubes." This response added strength to the decision to continue the in-house build of the monitor. Although the high resolution CRT is still considered a single-source item, the remaining electronics are widely available to Sperry Univac.

2.2 MONITOR SYSTEM

A block diagram of the Univac-built color monitor is shown in Figure 2.1. The monitor contains a high resolution color CRT, a deflection yoke with its horizontal and vertical drivers, a convergence yoke with its driver, a purity and blue lateral assembly, a video amplifier, and power supplies for producing the anode and focus voltages.

The signal inputs to the monitor are separate horizontal and vertical syncs, separate R, G, and B data and video, horizontal, and vertical addresses, and control for the video amplifier. The syncs, data, video, addresses, and control signals are low level, $\approx$ 5 volt, signals with a bandwidth of 20 MHz.

The power inputs to the monitor are +115, +48, +24, +12, +5, and -16 VDC and 115 VAC. Total input power increases with the display intensity to a maximum of about 85 watts.

The construction of the monitor is modular. The horizontal, vertical, focus, convergence, and video amplifier assemblies are contained on individual, removable circuit boards. Any individual assembly can be removed and the remainder remains operable. The focus and high voltage power supplies are separate assemblies. The deflection and video electronics can be operated without having the high voltage operable. This feature and the modular construction facilitates maintenance.

2.2.1 CRT Characteristics

The CRT used in the monitor is a 13 inch diagonal, 90° high resolution tube built by Matsushita. This tube has three guns arranged in a delta configuration with a conventional, circular-opening shadow mask and round phosphor dots. The mask contains 690,000 dot trios on a center-to-center spacing of 0.012 inch. This is a dot density of about three times that of a conventional color CRT. The raster size is 10.9 by 8.1 inches maximum. The data and video are presented over an area of 9.3 by 7.0 inches. This underscan provides optimal linearity, purity, and convergence over the viewing area. The 15 inch diagonal tube can also be used in the monitor with no change to the electronics. The display area is then 10.6 by 7.9 inches with slightly increased resolution due to the 910,000 dot trios in the 15 inch tube.

The resolution of either tube is sufficient to display a character matrix of 80 characters per row by 24 rows or 1920 characters. The total dots which can be displayed are 640 by 480 or 307,200 dots on a 525 line interlaced display. Thus, each character dot occupies two to three phosphor dot trios.

The anode voltage required is 25 KV nominal at 500 $\mu\alpha$ maximum. If the beam currents are increased above 500 $\mu\alpha$ total, the three beams tend to "bloom" and defocus. The relatively low beam currents used are adequate to maintain brightness consistent with resolution.

The focus voltage must be variable between 4.5 to 6 KV to provide proper focusing. A dynamic voltage of about 300 volts peak should be superimposed

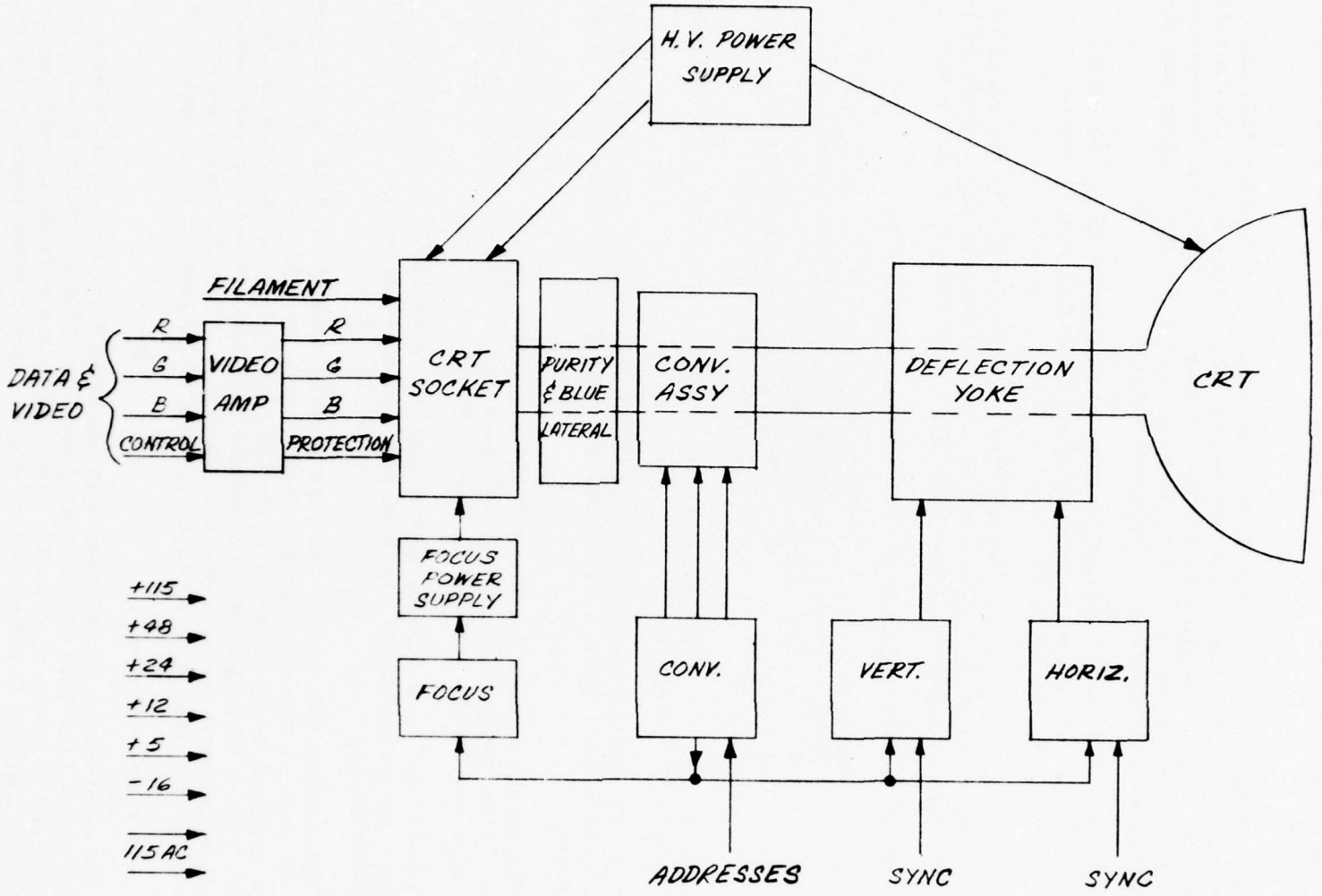


Figure 2.1 Color Monitor Block Diagram

on the focus voltage. In the present monitor, this voltage is varied at both the horizontal and vertical rates to provide an optimum focus over the entire display area.

The second grid or G2 voltage must be adjusted to between +200 and +1000 volts. This voltage varies due to the characteristics of the individual guns and tubes. The maximum voltage to which the grids can be adjusted is controlled and is used to limit the beam current to about 150 μa per gun. This limit then functions as a brightness limiter.

The first grid or G1 voltage must be varied from -10 to -60 volts. Making this grid more negative decreases the intensity and is used as the intensity control for the monitor.

The cathode voltages are varied from +5 to +40 volts by the video amplifier. The data and video information is used to modulate the cathode voltages. The beam is essentially cut off when the cathode is at +40 volts.

Nominal voltages for the present 13 inch monitor are:

Anode	25.0 KV
Focus	5.9 KV with 250 volts dynamic
G2	+300 volts
G1	-30 volts at nominal intensity
Cathode	+5 to +40 at video rate

Manufacturer's data on the tube gives tolerances which dictate the voltage ranges quoted previously.

The CRT requires magnetic fields to perform corrections on the individual electron beams. These corrections are called purity, blue lateral, and convergence.

The purity magnets provide a field adjustable both in magnitude and direction. This field is applied to all guns and is used to center the beams and to give the proper trajectory to each beam.

Ideally the blue lateral magnet provides a vertical field only to the blue gun. This field moves the blue beam horizontally and is used to obtain proper convergence.

The convergence magnets and yoke provide separate fields, static and dynamic, to each of the three guns. These fields must be varied at the horizontal and vertical sweep rates to cause the three beams to converge on the same phosphor trio. The magnitude and waveshape of the corrections vary between guns since the guns are in a delta arrangement. Thus the three beams do not originate at the same spot or have the same trajectory to the phosphor screen.

2.2.2 Convergence System

The convergence system generates and controls three separate parabolic currents which flow through the red, green, and blue convergence coils arranged around the neck of the CRT. These currents provide to each gun the appropriate magnetic field needed to achieve proper convergence of the beams over the entire display area. A block diagram of the system is shown in Figure 2.2.

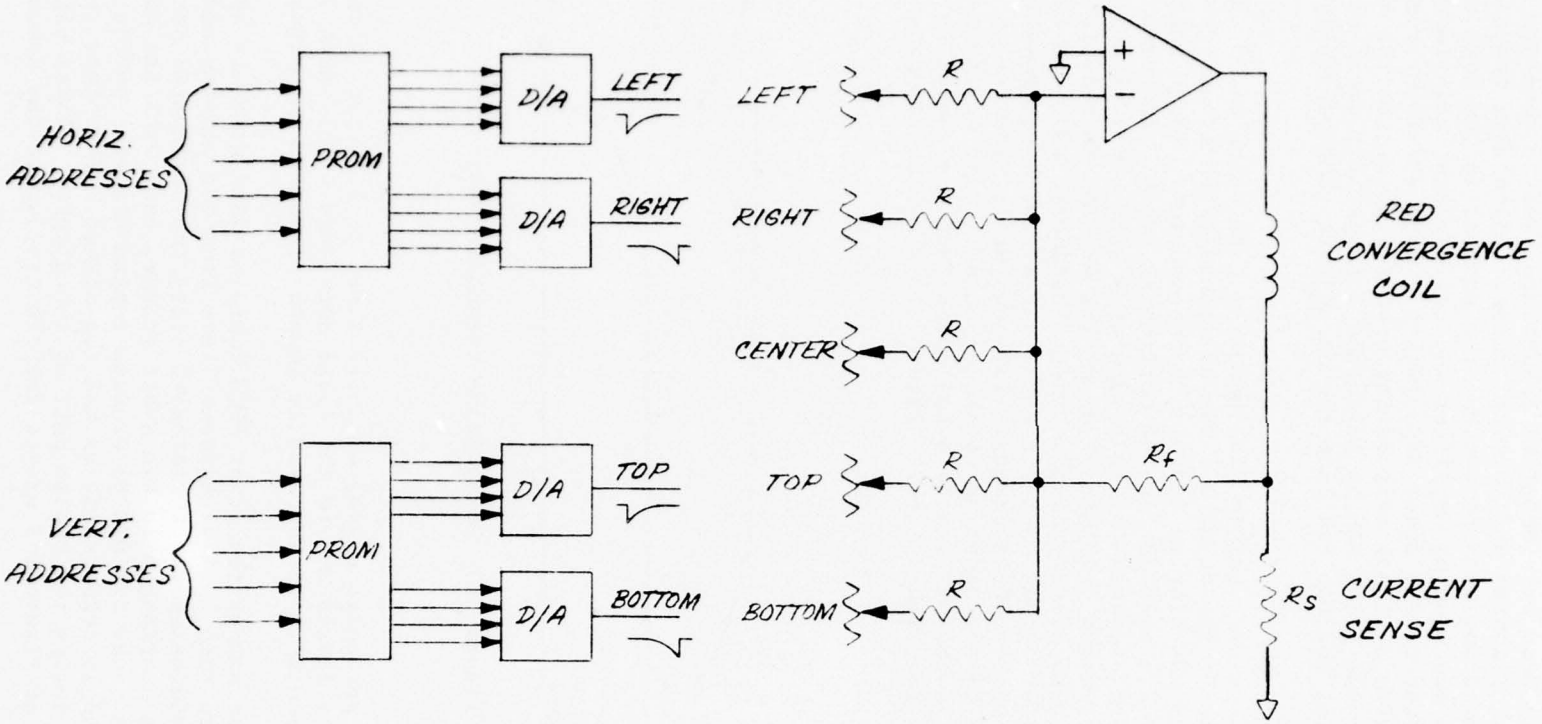


Figure 2.2 Convergence System

Programmable Read Only Memories (PROM) are used to generate parabolic waveforms at the horizontal and vertical rates. Adjustable fractions of these waveforms are summed and used to control the current in the coil of each gun. Each beam has its own summing amplifier and coil so that adjustment for each color is independent of the other adjustments. Each waveform from the PROM is chosen to provide a signal only during specific points on the sweep so that adjustment to any one color can be performed for specific areas of the display. For example, the top red beam can be adjusted independently of the left green beam.

The PROMs used are fusible link memories consisting of 32 addresses which each produce 8 bits of data. The horizontal PROM is addressed by five address lines from the display address column counter. These addresses are incremented every 2.5 μsec during the horizontal sweep. The data contained within the PROM are arranged in two groups of 4 bits each. Each group has its own D/A converter, which consists of an R, 2R, 4R, and 8R resistor network. The data in one group are arranged so that a parabolic waveform is produced at its D/A converter output every time the horizontal sweep moves from the beginning to the center of its sweep. This output is referred to as the left signal. The data in the other group produce a parabolic waveform from its D/A converter while the horizontal sweep moves from the center to the end and is referred to as the right signal. Figure 2.3 shows the signals with respect to time.

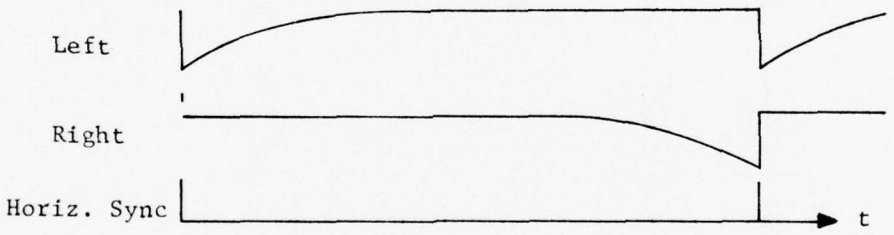


Figure 2.3 Convergence Parabolic Waveform

The actual parabolic signal exhibits steps at 2.5 μsec increments and one of 16 possible levels due to the 4-bit data word. This granularity is fine enough to result in an essentially smooth parabolic convergence current.

In a similar manner the other PROM contains data which is addressed at the vertical sweep rate by five address lines from the display address row counter. These addresses are incremented every ten horizontal sweeps or 635 μsec. The data are arranged in two 4-bit groups, each with its own D/A converter. The data cause one D/A to produce a parabola only during the top half of the display and is referred to as the top signal. The other group and D/A produce a signal during the bottom half of the display. These signals are similar to those of Figure 2.3 except for the time scale and nomenclature.

The granularity of the vertical signals is noticeable and so capacitive smoothing is performed on the vertical D/A outputs.

These four parabolic signals are applied to three separate amplifiers to produce completely independent red, green, and blue convergence currents. Figure 2.2 refers to the red amplifier, but the green and blue amplifiers are identical and share the same four parabolic signals. These four signals are also used for linearity, pin cushion, and dynamic focus corrections.

Each parabolic signal is applied to its respective adjustable divider. The outputs of each divider are summed together in an inverting amplifier. The feedback network of the amplifier responds to the convergence coil current so that the current is the sum of the fractions of the left, right, top, and bottom signals as adjusted by their individual dividers. In addition, a center voltage is summed to provide for convergence in the center of the display, i.e., static convergence.

The convergence coil current is given by Equation 1:

$$I_{coil} = \frac{R_f}{R_s R}\left[V_{Left} + V_{Right} + V_{Top} + V_{Bottom} + V_{Center}\right] \qquad (1)$$

where V_{left}, V_{right}, V_{top}, V_{bottom}, and V_{center} are the voltages adjusted by each respective divider. The coil current thus consists of a static level, a parabola at the horizontal rate, and a parabola at the vertical rate. These parabolas may be skewed depending on the setting of the dividers. The horizontal and vertical currents are summed in one coil rather than applied to separate coils as in a conventional system.

Figure 2.4 shows the blue convergence current.

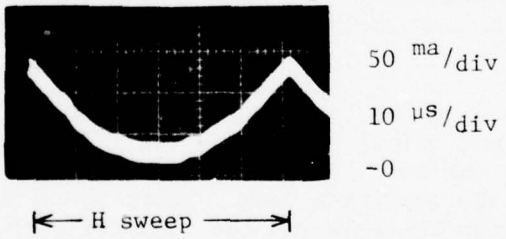


Figure 2.4 Blue Convergence Current (Horizontal)

The horizontal parabola is evident together with modulation caused by the vertical component. A centering level of 15 ma is seen as a displacement from the zero axis.

The blue convergence current envelope during a vertical sweep is shown in Figure 2.5

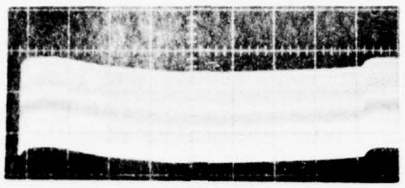


Figure 2.5 Blue Convergence Current (Vertical)

There is more current during the top of the sweep than during the bottom since the blue gun is aimed slightly downward and so requires more correction at the top.

Power required for the convergence assembly is +48, +24, and +5 volts at a total of about 8.5 watts. Note that no power is taken from the horizontal or vertical yoke currents or flyback pulses, as is conventional. (The usual convergence system uses these yoke currents and pulses together with passive networks to generate the necessary parabolic currents.)

Using this technique, convergence of the 13 inch or 15 inch CRT takes less time and is more accurate over the entire display area than the traditional method. The data in each PROM has been tailored to give the exact correction required at all areas of the display. Each color can be moved in specific sectors of the display and independently of the other two colors. There is none of the cross talk between areas or colors evident in conventional methods. Convergence in one area does not cause misconvergence in another area, and so it is not necessary to converge repetitively, as is usually the case.

The controls on the convergence assembly are laid out to relate to the specific sector and color. Adjusting the left-hand blue control only moves the blue beam in the left side of the display. Similarly, the top green control only moves the top green beam. Thus, there is a relationship between the location of the controls and the respective sector and color which they control. This and the lack of interaction result in a 30 second convergence of the CRT.

2.2.3 Horizontal Sweep System

The horizontal sweep system uses a flyback yoke drive with a phase locked loop to synchronize the sweep current to the external horizontal sync. The supply voltage to the yoke is adjustable for width control and is modulated at the vertical rate for side pin cushion correction. Figure 2.6 is a block diagram of the horizontal sweep system.

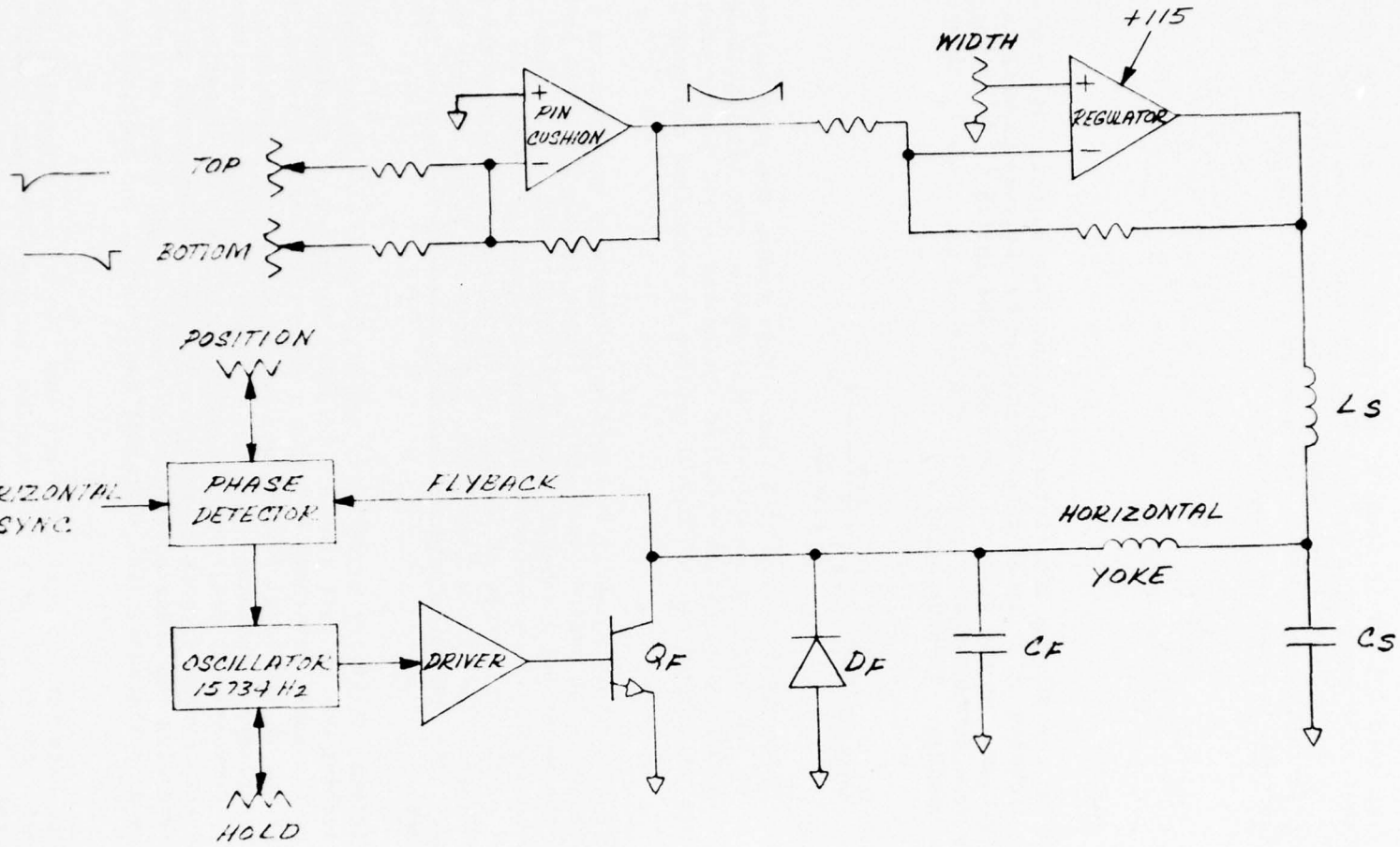


Figure 2.6 Horizontal Sweep System

The saddle yoke used for the 13 inch CRT has an inductance of 1.3 mh and requires a current of 4 amp p-p to deflect a 25 KV beam a total of 79° (90° diagonal). The 15 inch CRT yoke has identical electrical characteristics and can be used with this sweep system. For a sweep time of 55 μsec the supply voltage to the yoke is given by Equation 2:

$$V_s = L_{yoke} \frac{I_{p-p}}{t_{sweep}} \tag{2}$$

and is 94.5 volts.

Turning on the flyback transistor Q_F causes the sawtooth yoke current or ±2 amp to increase at a linear rate determined by the yoke inductance and the supply voltage. At the start of the flyback the switch Q_F is abruptly opened. The yoke current then flows into the flyback capacitor C_f charging it to a peak voltage. (See Equation 3.)

$$V_{Flyback} = \frac{\pi}{2} L_{yoke} \frac{I_{p-p}}{t_{retrace}} + V_s \tag{3}$$

of 1,114 volts for a retrace time of 8 μsec. This causes the yoke current to reverse direction and initiate a new horizontal sweep. The damping diode D_F conducts this current until slightly before the center of the raster when Q_F is again turned on. These are 1,500 volt devices to withstand the peak flyback voltage.

The yoke current is slightly S-shaped as a result of modification of the source voltage. The source capacitor C_s charges during the first or left-hand half of the sweep and discharges during the right-hand half. This charge and discharge by a current ramp produces a parabolic voltage of about 20 volts peak on the capacitors at the center of the raster superimposed on the supply voltage. The source inductance L_s forces the sweep current into the capacitor. This S-shaping procudes a linear sweep of the beam on the phosphor screen.

No additional linearity corrections are performed. The raster exhibits a slight stretching on the left side and a slight shrinkage on the right. This is due to the yoke resistance of about 1 ohm which causes the yoke current to change not at the ideal linear rate but slightly exponentially. The amount of stretching and shrinkage is about 1/8 inch, which is not noticeable at the edges. Conventional sweep systems usually require some linearity correction since they have a flyback transformer and convergence circuitry which requires power during the trace portion of the sweep. This power is reflected in the yoke as resistance which increases nonlinearity and requires correction.

The phase detector and oscillator are combined in one integrated circuit. The oscillator is set at a free running frequency of about 15,734 Hz by the hold control. Thus the sweep will operate in the absence of an external sync. The phase detector compares the phase between the sync and a sample of

the flyback pulse and produces a static voltage proportional to the phase difference. This voltage controls the oscillator frequency in order to maintain zero phase difference. The position control changes the phase of the flyback sample in the detector and thus can be used to change the phase relationship of the flyback with respect to the sync. This does not move the raster on the CRT but only moves the data on the raster. The hold control also functions similarly to the position control. The combination of these two can move the data on the raster about $\pm$1/2 inch or 2.5 µsec with respect to the sync. This is sufficient to center the data and video on the display area. The purity magnets function as a centering adjustment to center the raster on the CRT screen.

The hold-in range of the phase-locked loop varies between integrated circuits but averages about $\pm$10% of the center frequency. The pull-in range is about $\pm$5%. Thus, the horizontal sweep system should lock and hold onto sync over a frequency range of 14,950 Hz to 16,520 Hz, well within the $\pm$1% tolerance allowed by the RS-170 standard. The measured jitter of the sweep current with respect to the sync is about 20 nsec. This corresponds to about 1/4 of a character dot (80 nsec) and is not apparent when viewing data or video. Figure 2.7 shows the horizontal yoke current and the sync pulses. The slight S-shaping is evident.

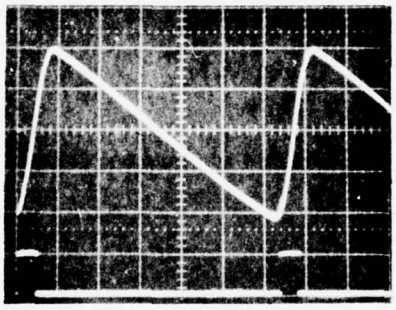


Figure 2.7 Horizontal Yoke Current and Sync Pulses

The oscillator output is amplified and shaped by the driver, which supplies base current to the flyback transistor Q_F. The amplitude and shape of the drive current has been chosen to minimize power dissipation in the transistor.

The supply voltage to the yoke is controlled by a feedback amplifier denoted regulator in Figure 2.6. One input to the amplifier is an adjustable voltage which controls the yoke static voltage and serves as the width control. The other input is an adjustable parabola at the vertical sweep rate. This modulates the yoke voltage by decreasing it at the top and bottom of the raster to compensate for side pin cushion distortion. The modulated supply voltage is coupled to the yoke through a relatively small, $\approx$10 mh, inductance L_S. A larger inductance would cause a phase shift between the supply voltage from the regulator and the yoke voltages and so the desired pin cushion correction would not be performed at the proper time during the vertical

sweep. If the supply voltage were coupled to the yoke at the flyback transistor as usual, a much larger inductance would be required to withstand the peak flyback voltage. The present inductor must only withstand the relatively small S-shaping voltage. This large inductance would not allow modulation of the yoke voltage for pin cushion correction. The present arrangement is feasible since no flyback transformer is used for high voltage generation.

The pin cushion feedback amplifier sums the top and bottom signals from the convergence assembly in adjustable portions to generate a vertical parabola for application to the regulator. Thus, the side pin cushion correction can be performed independently for the top and bottom of the raster.

Figure 2.8 shows the envelope of the horizontal yoke current during the vertical sweep.

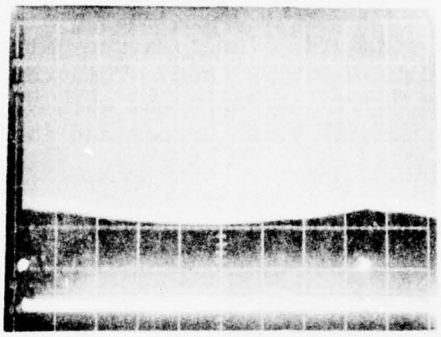


Figure 2.8 Horizontal Yoke Current During Vertical Sweep

The current varies from 4 amp p-p at the center of the raster to 3.8 amp at the top and bottom. This reduction of 5% is sufficient for adequate side pin cushion correction.

Power required by the horizontal sweep system is 115 volts at 100 ma and 24 volts at 190 ma for a total of 16 watts. Power dissipation in the yoke is 1.7 watts and about 6 watts in the flyback transistor. The remainder of the power is dissipated largely in the regulator and driver.

The horizontal system also contains protection circuitry for the CRT. The horizontal and vertical flyback pulses are detected and converted to a logic level. If either pulse is absent, the video amplifier is turned off and the guns cut off. This prevents phosphor burn in the event of a loss of sweep since, with no flyback transformer, the high voltage is present even with no sweep.

2.2.4 Vertical Sweep System

The vertical sweep system uses a linear feedback amplifier to drive the vertical yoke. The yoke current is equal to the sum of sawtooth, linearity, and position inputs. Top and bottom pin cushion corrections are coupled to the yoke separately from the amplifier. Figure 2.9 is a block diagram of the vertical sweep system.

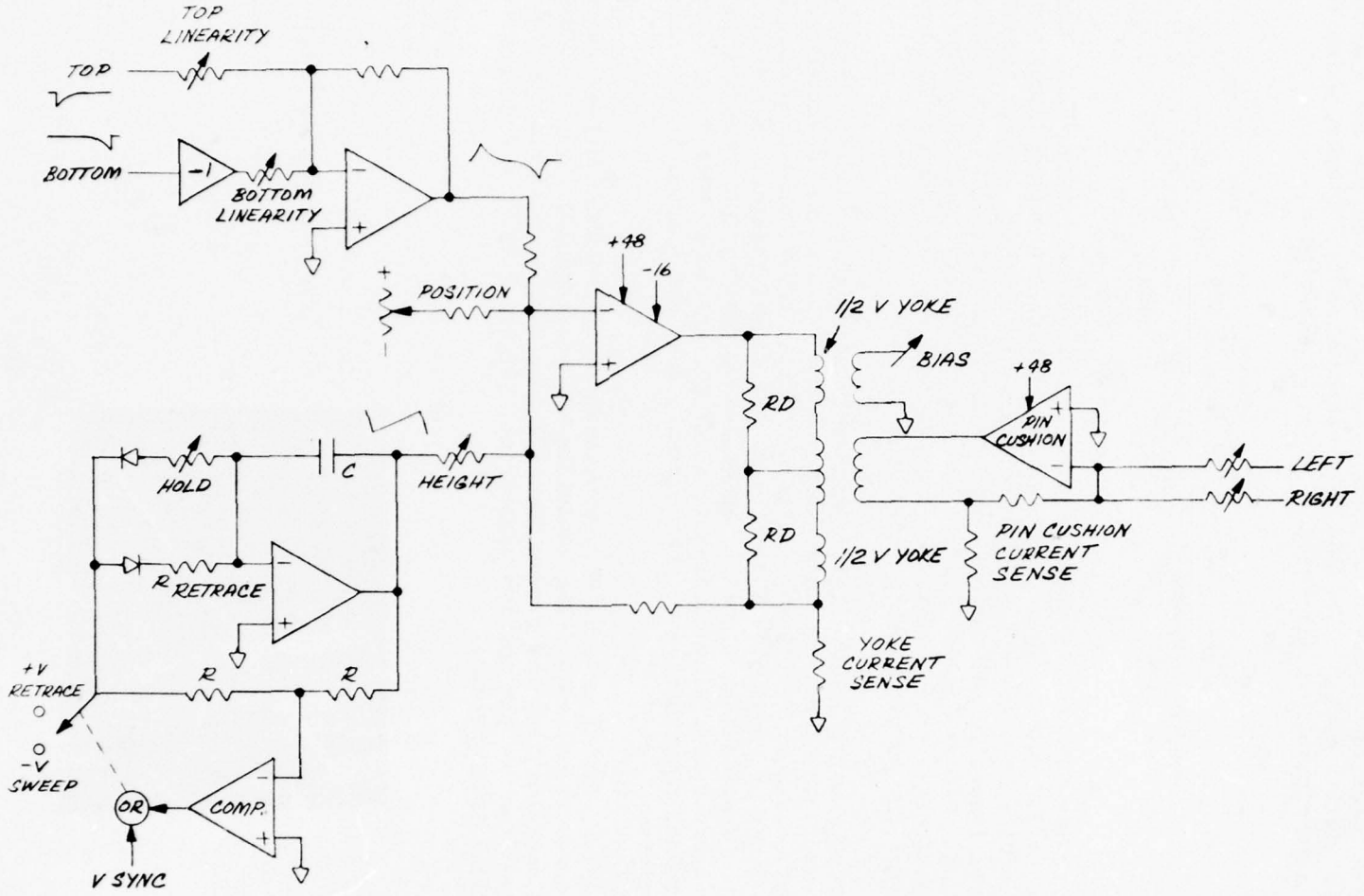


Figure 2.9 Vertical Sweep System

The vertical yoke is split into two windings with a total inductance of 42 mh and a total resistance of 23 ohms. The current required for a deflection of 60° is 540 ma p-p. The nominal retrace time is 750 μsec, which requir requires a supply voltage for retrace, given by Equation 4,

$$V_{\text{Retrace}} = L_{\text{Vertical}} \frac{I_{p\text{-}p}}{t_{\text{retrace}}} + \frac{I_{p\text{-}p}}{2\ R_{\text{yoke}}} \qquad (4)$$

of 36 volts for the present yoke. The voltage required for the sweep time of 15.9 msec is 7.7 volts. These requirements dictate the voltage range which the yoke amplifier must supply. The voltages are slightly greater than these to overcome losses in the current sense resistor and pin cushion transformer. The vertical yoke is directly coupled to the amplifier. Thus, no bulky coupling capacitor or transformers are required and the yoke current can have a static level for vertical centering of the raster.

The yoke amplifier has three separately adjustable inputs. These are a linear sawtooth, which controls the sweep and retrace and is varied for raster height; a static level, for position control; and a quasi-parabola, for vertical linearity control. These inputs are summed together in a feedback amplifier. The feedback signal is generated by sensing the yoke plus damping resistor R_D currents. The damping resistor current is at most 7 ma; this small current, compared to the yoke current, does not cause any discernible nonlinearities.

The yoke amplifier uses an operational amplifier which drives complementary power transistors. The bandwidth has been reduced to about 2 KHz to optimize settling time and prevent oscillations at the horizontal rate due to excitation from the pin cushion correction. Figure 2.10 is a photograph of the vertical yoke current.

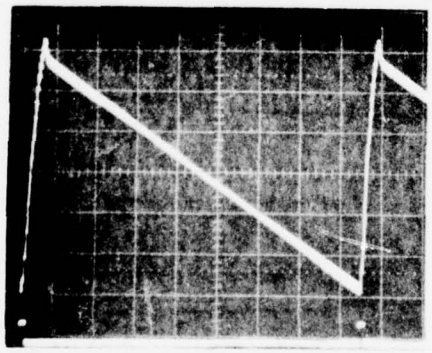


Figure 2.10 Vertical Yoke Current

The sawtooth generator consists of an integrator which is reset either by an external vertical sync or by an internal comparator. It will free run until locked by the sync.

The output voltage (sawtooth) of the integrator is given by Equation 5.

$$V_{saw} = -\frac{1}{C} \int I \, dt \qquad (5)$$

The current to the integrator, I, is changed both in magnitude and direction during sweep and retrace. During sweep the current flows out of the integrator and is determined by the hold resistor. This current causes a linearly increasing sawtooth voltage. The rate of increase can be adjusted by the hold control and sets the free running frequency. During retrace the current flows into the integrator and is determined by the retrace resistor. (Refer to Figure 2.9.) This larger current causes the sawtooth to decrease at a faster rate and complete retrace in about 750 µsec.

The integrator current is changed by a switch controlled by either an external sync or an internal comparator. When the sawtooth voltage has risen to a level of V volts in the absence of a sync, the comparator will switch the current to the +V source, thus initiating retrace. When the sawtooth has decreased to -V volts the comparator will switch the current to the -V source, initiating the sweep portion of the vertical cycle. Thus, the sawtooth consists of a linear ramp having peak voltages of $\pm$V.

If a sync pulse is present, it will initiate the retrace. Once the retrace is started the comparator will complete the retrace and start the sweep. The only restriction is that the sync pulse has less width than the retrace time.

The free running frequency is set by the hold adjustment at slightly less than 59.94 Hz. At that rate the sync pulses will occur slightly before the free running retrace and will initiate retrace. The vertical sync pulses are generated in the control logic by sensing the first serration of the composite sync. Thus, the vertical syncs presented to the sweep system vary exactly 1/2 a horizontal sweep between even and odd fields. The vertical retrace is initiated exactly in time with the sync since there is no smoothing or integration of a composite sync. The sawtooth always reaches the same voltage level during retrace regardless of the even or odd field. Thus, the yoke current and the raster always return to exactly the same point at the end of retrace. This results in a perfect interlace with no adjustment necessary.

The linearity corrections are performed by using the top and bottom signals from the convergence assembly to modify the yoke current. The bottom signal is inverted and then added to the top signal in a summing feedback amplifier. Both top and bottom signals can be adjusted individually. This adjustable quasi-parabolic signal at the vertical rate is added to the sawtooth and position signals at the yoke amplifier. Figure 2.9 shows the circuit configuration and the signals. The parabola rounds the ends of the

sawtooth into an S-shaped signal which controls the yoke current. The S-shaped current produces a linear vertical sweep of the beam on the CRT screen.

The top and bottom pin cushion correction is performed by superimposing a variable amplitude and polarity horizontal parabola onto the vertical yoke current. The parabolic correction must have maximum amplitude at the top and bottom of the raster, zero at the center, and change polarity between top and bottom. The correction reduces the vertical yoke current at the start and end of each horizontal sweep and so pulls in the corners to obtain a rectangular raster. Magnets cannot be used for this correction as they are in monochrome monitors since the magnets would affect purity and convergence. The envelope of the pin cushion modulation of the yoke current can be seen in Figure 2.11. The change in amplitude with vertical sweep is evident. A photograph of the top and bottom portions of the yoke current on an expanded time scale is shown in Figure 2.11.

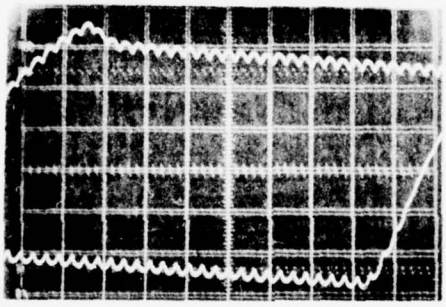


Figure 2.11 Top/Bottom Yoke Current

The change in polarity of the correction can be seen.

The pin cushion correction currents are coupled to the vertical yoke by a saturable transformer. The amount and phase of the coupling is determined by the degree and area of saturation of the ferrite transformer core. The transformer is driven by a parabolic current generated by a summing feedback amplifier. The inputs to the amplifier are signals from the convergence assembly that can be adjusted from left to right. Thus the pin cushion correction can be performed independently for the left and right sectors of the raster.

The transformer is a three-leg ferrite core with drive and bias windings on the outer legs and secondary windings on the center leg. The correction currents induced in the secondary flow through each half of the vertical yoke and return through the damping resistors. Thus, this current does not flow in the yoke amplifier or yoke sense resistor and does not interfere with the sawtooth current but is superimposed on it. If the yoke amplifier had to supply the pin cushion current the voltage and frequency requirements on it would be severe.

A diagram of the saturable transformer is shown in Figure 2.12.

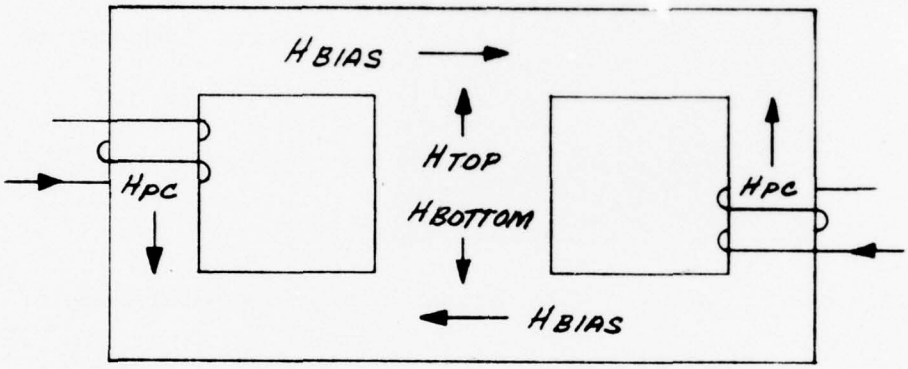


Figure 2.12 Saturable Transformer

A bias field is applied around the outer legs by windings (not shown) through which the current can be varied. The bias field is normally half that required to saturate the ferrite in the outer leg. The field produced by the center winding due to the sawtooth yoke current is also about half of saturation when the yoke current is a maximum at the top and bottom of the raster. At the top of the raster this field plus the bias field saturates the right leg and the left leg becomes unsaturated. Then the pin cushion winding on the left leg is completely coupled to the secondary winding on the center leg and produces the maximum correction at the top of the raster. As the yoke current decreases, the coupling decreases and the core goes toward saturation, and so the correction decreases. At the center of the raster the left and right pin cushion windings couple equally but out of phase to the secondary producing zero correction. At the bottom of the raster the right winding couples maximally but in the opposite phase, producing the corrections shown in Figure 2.11.

The amount of coupling as a function of yoke current can be varied by the adjustable bias current. This is done to produce the desired "butterfly" modulation evident in Figure 2.10 and so obtain the proper correction over the entire raster. This modulation is denoted by the widening of the trace of the top and bottom of the sweep.

The pin cushion correction is a parabola at the horizontal rate. Figure 2.13 is a photograph of the vertical yoke current during a horizontal sweep. The parabolic current contrasts with the conventional method, which uses a sine wave current generated by tuning and phasing the flyback pulse. This sine wave leads to a slight upturn, i.e., insufficient correction, at the corners of the raster which does not occur in the present monitor.

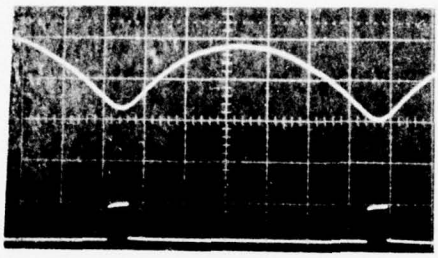


Figure 2.13 Vertical Yoke Current During Horizontal Sweep

The power required by the vertical system is +48 volts at 133 ma, +12 at 20 ma, -16 at 106 ma, and +5 at 170 ma for a total of 9.2 watts. About 3 watts is used in the pin cushion amplifier and driver, 4 watts is dissipated in the complementary output transistors of the yoke amplifier and about 2 watts in the yoke.

2.2.5 Focus System

The focus voltage required by a 13 inch or a 15 inch CRT must be adjustable from 4.5 to 6 KV to obtain optimum focus. This voltage must be modulated to slightly increase the focus voltage at the edges of the raster. This modulation (dynamic focus) is about 200 volts at the horizontal rate and 110 volts at the vertical rate.

The monitor uses a commercial high voltage supply to provide the adjustable static voltage. This supply and its 24 volt power source are isolated from ground. The entire supply and source are driven about 310 volts from ground by the dynamic voltage source. The block diagram of the focus system is shown in Figure 2.14.

The dynamic amplifier is a feedback summing amplifier which has inputs from the left, right, top, and bottom convergence signals in the proper proportions. The output of this amplifier drives a 1:20 ratio transformer, and its secondary develops the dynamic focus voltage. The left and right signals

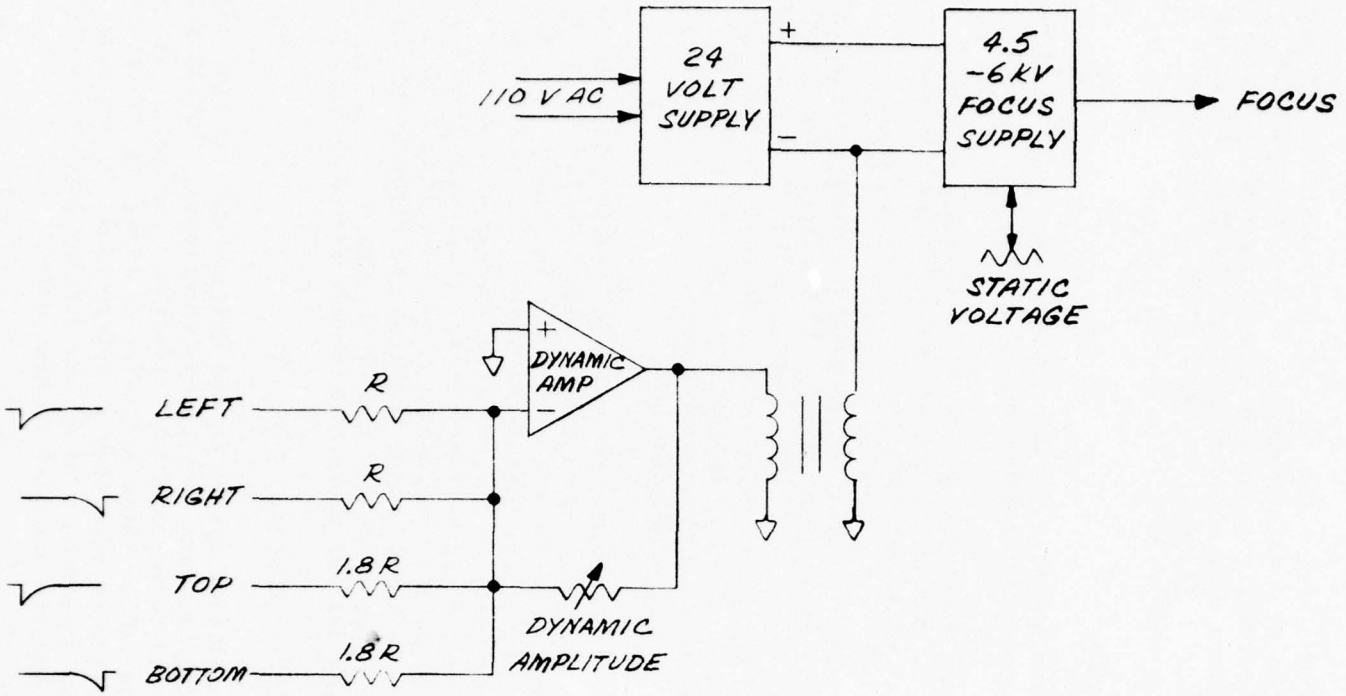


Figure 2.14 Focus System

provide a nominal 200 volt peak horizontal parabola. The top and bottom signals provide a nominal 110 volt peak vertical parabola. The composite dynamic voltage can be varied in amplitude by a control in the feedback loop to obtain optimum focus over the entire raster.

The ratio of the horizontal to vertical corrections is about 1.8:1 and is determined by the R, 1.8R arrangement of the inputs to the amplifier in Figure 2.14. The dynamic voltage required is a parabola or varies with the square of the distance from the center of the raster. Since the aspect ratio of the raster is 4:3, horizontal to vertical, the ratio of the components of the dynamic voltage should be $(4/3)^2$ or 1.77.

2.2.6 Socket Assembly

The CRT socket assembly contains spark gaps, adjustable controls for the grids, and protection for the phosphor.

The spark gaps are essential to allow internal arcs from the high voltage to be shunted to ground and not arc to the cathodes, which would result in a failure of the video amplifier.

Separate adjustable controls are used for each gun for both grids. The G2 voltage can be adjusted from +200 to +1000 volts. The G1 voltage can be varied from -10 to -60 volts. The three G1 voltages are derived from a common variable voltage, which is used as the intensity control for the monitor. The G1 and G2 voltages are initially set to obtain, in the absence of any video, a white raster which tracks or remains white as the intensity is varied from minimum to full brightness.

The socket also contains protection circuitry, which is vital to protect the CRT phosphor. If there is a loss of either horizontal or vertical sweep the video amplifier is turned off. However, if the low voltage supplies should fail, this protection is not available. The cathodes will be at ground potential or fully on and the high voltage will still be on since it is not generated by a flyback transformer. To prevent phosphor burn in this situation a reed relay is used to switch the G2 voltage. This relay is activated by the +48 volt supply which supplies the video amplifier. If this supply fails, the relay opens and the G2 voltage at the grids drops to zero, effectively cutting off the beams even though the cathodes are fully on.

2.2.7 Video Amplifier System

The video amplifier system in the Univac-built monitor combines internally generated digital data (dot-bar pattern) with external signals from the display and develops voltages which drive the three guns. The block diagram is shown in Figure 2.15. There are three of these amplifiers in the monitor. They are not complete in that they do not receive and mix video data or generate half saturation graphics as do the display amplifiers discussed in Section 6, but they operate and perform similarly.

The cathode of the R, G, or B gun must be driven between +5 volts of full intensity to +40 volts at cut off. The driver is a linear amplifier which develops this signal in response to internal or external signals.

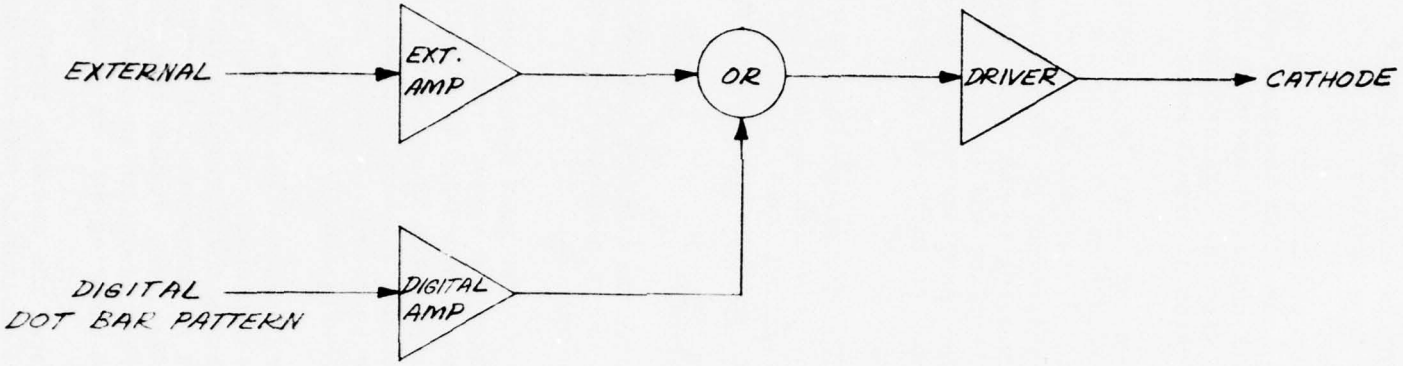


Figure 2.15 Video Amplifier System

The digital amplifier receives signals indicative of the dot or bar pattern. This signal, common to all three amplifiers, is converted to a current of 68 ma. This current is ORed with the external signal and can drive the cathode via the driver to a cathode voltage of +5 or +40 volts.

The external amplifier can also drive the cathodes independently of the digital data. The external amplifier receives separate R, G, and B signals at a 1 volt p-p level (black negative) and develops a current of 68 ma maximum. This current is ORed with the digital current, if any, and drives the cathode linearly with the external signal input.

The driver is a common base amplifier. Either digital or external signals can supply the emitter current. The current ORing is done at this low impedance point to minimize voltage swings and maintain the frequency response. Either signal is sufficient to fully drive the amplifier. The amplifier is prevented from saturating in the simultaneous presence of both signals by the use of diodes to clamp the collector voltage. The voltage at the collector is buffered by complementary emitter followers to provide a low impedance source to the cathode so that the cathode capacitance (15 pf) may be driven at the video rates.

The frequency response of the amplifier is 17 MHz and is shown in Figure 2.16. This results in a risetime at the cathode of about 20 nsec. Since each dot displayed is 80 nsec wide, this risetime is essential to prevent smearing of the visual data and maintain resolution.

2.2.8 High Voltage Power Supply

The high voltage source used in the monitor is a commercially regulated 25 KV power supply. This source also supplies regulated +1000 volts and -60 volts for use in the grid controls.

The high voltage to the CRT must remain constant since the load on it changes when the raster intensity varies from zero to maximum. The total beam current goes from zero to about 500 μa when the data on the CRT are blinked. If the voltage regulation is not sufficient, the raster size will change as the data is blinked. The high voltage must be regulated to within 2% to maintain raster size to within .1 inch. Thus, the 25 KV supply output must change less than 500 volts from no load to full load.

A flyback transformer high voltage system cannot maintain this regulation. Typical changes with intensity on the Matsushita monitor were 1,500 volts. That monitor decreases the horizontal yoke current as the high voltage is loaded in an effort to compensate. However, the vertical height increases with intensity. Also, the compensating feedback loop has a slow response which does not correct the width in phase with load changes. The change in raster size with blinking data is noticeable and distracting.

This situation dictated the use of a regulated high voltage supply. The load regulation of .1% maximum is more than sufficient to maintain constant raster size. The supply has sufficient current capacity, 1 ma, to power two tubes in a dual configuration. In addition, a flyback type of supply is not compatible with the horizontal sweep system described previously.

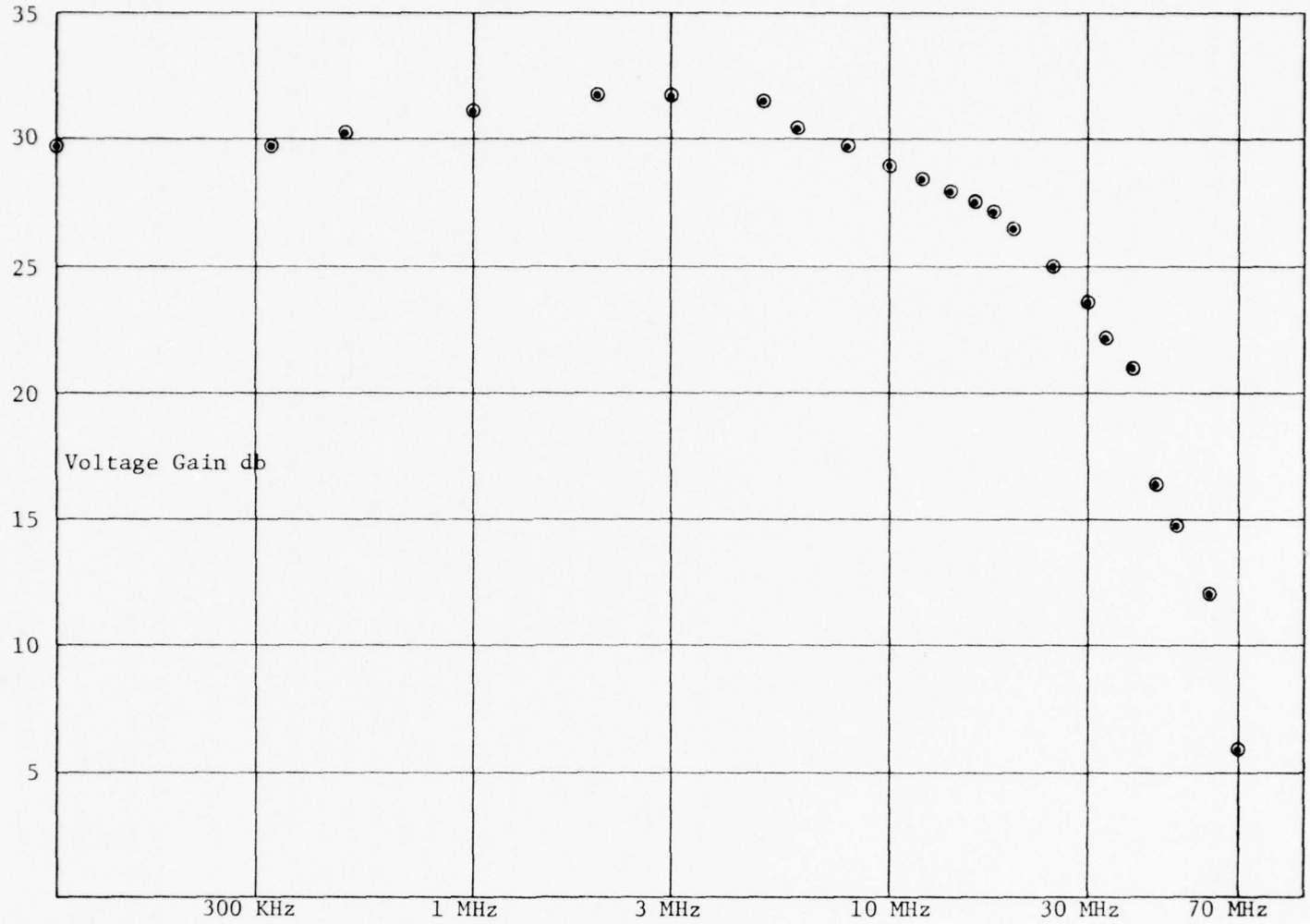


Figure 2.16 Video Amp Gain/Freq.

2.2.9 Monitor Power Requirement

The total power required by the Univac-built monitor is 85 watts for a full brightness raster and 58 watts with no raster. The supply voltages and maximum currents are listed in Table 2.1.

Table 2.1 Monitor Power Supply Requirements

Voltage	Current
+115 VDC	102 ma
+48 VDC	298 ma
+24 VDC	270 ma
+12 VDC	20 ma
+5 VDC	300 ma
-16 VDC	126 ma
115 VAC	420 ma

2.2.10 Monitor Packaging

The present packaging of the monitor is modular in that the horizontal, vertical, convergence, video, socket, and focus assemblies are contained on individual cards. The focus and high voltage power supplies are separately purchased items. The individual assemblies can be operated independently but do require correction signals from the convergence assembly. The low voltage power sources are common to the various cards.

The proposed packaging scheme utilizes one card for the horizontal and one for convergence, combines one for the vertical and focus, and uses four smaller cards for the video system. One sheet-metal assembly provides support and connections for the cards and has bulky components such as transformers and power transistors mounted on it. This assembly is complete and contains the entire sweep and convergence functions. The connections to this assembly are the syncs, addresses, power, and the deflection and convergence yokes. The video system is separate and has three identical cards for the R, G, and B amplifiers and one common control card to perform the saturation and video enables functions.

2.2.11 Alternatives and Recommendations

Alternatives which could be incorporated in future monitors to reduce cost and increase performance include:

a. Common focus supply
b. Stator yoke
c. Finer resolution of convergence waveforms

Presently, each monitor has its own focus supply (static and dynamic). Both monitors of a dual configuration could be driven from one static and one dynamic supply. (The present supplies have sufficient capacity to drive two

tubes.) This would separate high voltage (6 KV) dividers to adjust the static focus voltage independently for each tube from a common supply. The dynamic voltage from one supply could be separately adjusted for each tube and capacitively coupled to the static voltage to achieve the desired modulation. The trade-offs for a dual monitor are listed below:

Present	Proposed
a. Two focus supplies	a. One focus supply
b. Two dynamic supplies	b. One dynamic supply
	c. Two high voltage dividers
	d. Two high voltage capacitors

The yoke used in the present monitor is a high inductance, saddle wound yoke. The high inductance, 1.3 mh, requires the use of a relatively high voltage supply, which is used only in the horizontal system. This yoke exhibits aberrations in which certain areas of the raster cannot be converged to within less than .01 inch. As a result, white dots show some color fringing. A low inductance precision stator yoke may alleviate this misconvergence. Such a yoke could be driven from the +48 volt supply, which is required for other purposes. The lower flyback voltage of a stator yoke would allow use of lower voltage rating components. However, a low inductance yoke would require linearity correction which is not required at present. The trade-offs are:

Present	Proposed
a. 115 volt supply	a. Improved convergence
b. Slight misconvergence, no linearity correction	b. Linearity correction required
c. 1,500 volt devices	c. 600 volt devices

The present convergence system uses 20 horizontal and 24 vertical addresses to generate the parabolic correction waveforms. These result in a parabola which has 20 or 24 time steps. The horizontal steps are smoothed by the feedback amplifiers, which receive and manipulate the horizontal parabola, and so the correction waveforms at the horizontal rate exhibit little granularity. However, the 24 steps on the vertical parabolas cannot be smoothed without introducing undesirable phase shifts. These steps are evident in the side pin cushion correction as slight horizontal steps in a vertical line at the edges of the display area. The vertical linearity correction and convergence is not sufficient at the top-most row of displayed alphanumerics.

The convergence, linearity, and pin cushion corrections could be improved by increasing the vertical addresses from the present 24 to 48 during each vertical sweep to reduce the granularity of the vertical parabolas. This change would involve the use of a 64 x 8 PROM rather than the present 32 x 8 organization and a change to the display control logic to generate an extra address output (6 bits versus 5 at present).

2.2.12 Specifications

Tentative performance specifications for the Univac-built 13 inch diagonal monitor are:

1. Power consumption - 85 watts.

2. Display size
   a. 9.3 inch by 7.0 inch.
   b. Regulation - .2% line and load.

3. Geometric
   a. Distortion - display edges deviate less than .1 inch from ideal straight line.
   b. Linearity - deflected spot deviates less than 2.5% from its ideal position.

4. Convergence
   a. Performed independently for each color and independently for each sector of CRT.
   b. Time to converge - 2 minutes.
   c. Misconvergence - color fringing is less than .015 inch from ideal white dot.

5. Focus - single dot is less than .02 inch diameter over entire display area.

6. Video Amplifier
   a. Rise time - 20 nsec.
   b. Bandwidth - 17 Mhz at 3 db down.

3.0 CONTROLLER DESIGN

The controller used in the color demonstration module is similar to that used in the OJ-389(V) terminal. Figure 3.1 shows a detailed block diagram of the controller section.

The basic processing element is made up of the Intel 8080 microprocessor. Main communication paths are accomplished via a bus network. Included in it is the read bus which allows data bussed for the instruction and display memories to be made available to the Central Processor (CP). The write bus permits writing into the same memories as well as making data available to the I/O bus network. With the exception of these memories, all other subsections of the terminal communicate through the I/O bus network.

Addressing for various activities is accomplished via the address bus with the addressing originating from the CP. This addressing scheme provides the gating of data to the I/O port decode, both the instruction and display memories, the compare circuitry for cursor positioning, graphic control, and the sweep circuitry. The addressing generated by the display control and generation module provides for the addressing of the refresh memory during the refresh of the alphanumeric display data. Inputs to the sweep circuitry are used in addressing PROMs used in convergence of the color CRT, which is covered in Section 2 of this report.

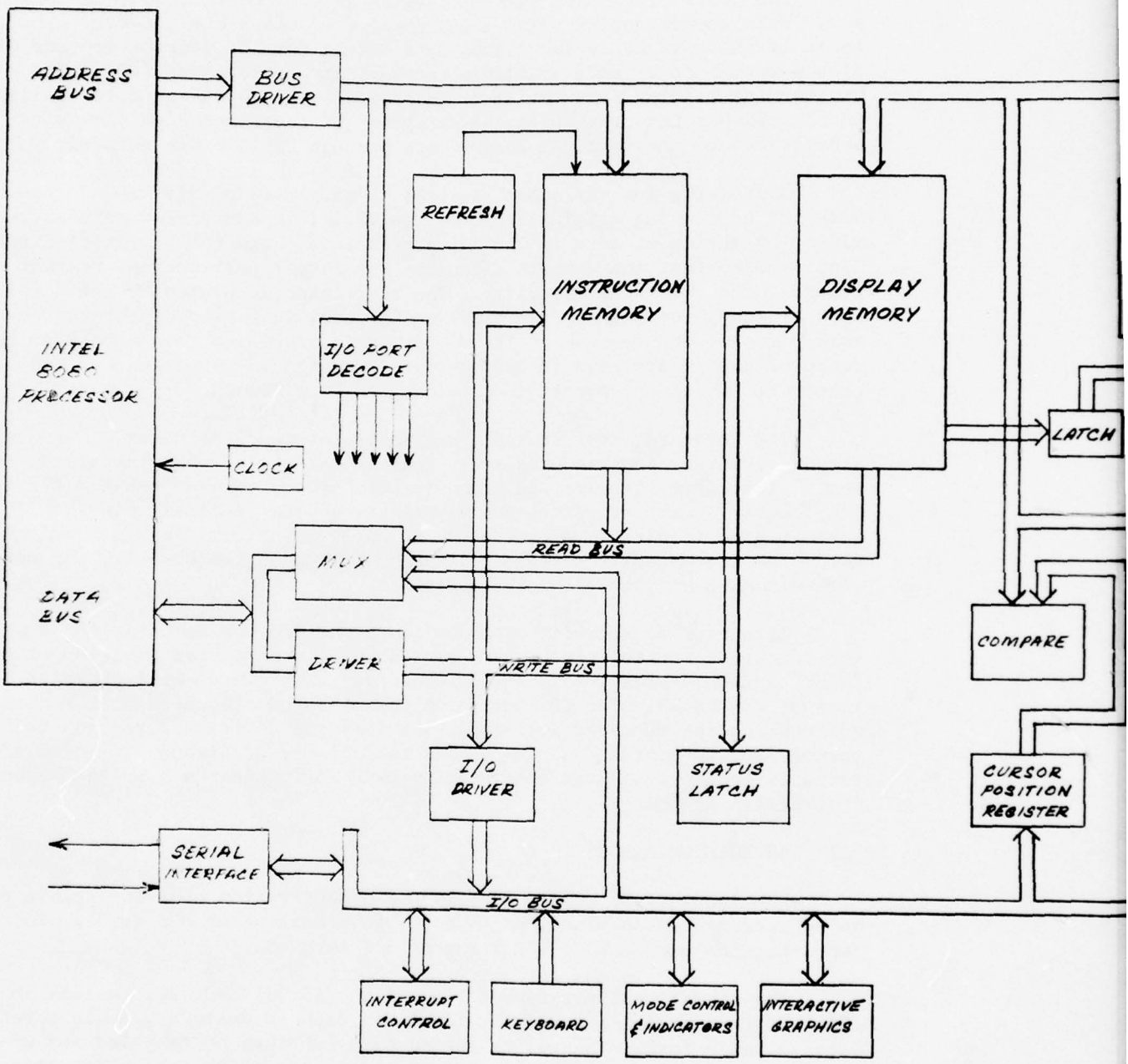
The keyboard, mode control, and indicator panel switches, interactive graphics, cursor position register, graphic data, and, when installed, the serial interface circuits all commonly communicate to and from the CP via the I/O bus. Each are independently addressed, as required, via the I/O port decode circuitry. Although not shown in the block diagram, communication with the magnetic tape unit is accomplished on the same I/O bus network via an 8-bit, parallel TTL interface.

Attention to activity by a device on the I/O bus is established by the interrupt control circuitry. For example, a completed function or "MARK" switch depression in the interactive graphic area will cause an interrupt to the CP. The CP, acting on the microcodes located at the entrance address for the received interrupt, services the device and returns to normal program operation. The CP has the ability to disable selected interrupts and lock out various functions and activities such as the keyboard, interactive graphics, etc.

3.1 INSTRUCTION MEMORY

The instruction memory used in the demonstration mode is capable of being incremented in size from 4K words to a maximum of 32K words. For demonstration purposes, the maximum of 32K is used.

The operational program, utilizing the 13,311 address, resides in this memory. The remaining memory available is used to capture graphic screen data in table form. The entire screen data can then be recalled for updating or restoring the graphic presentation, searching tables for presented screen data, or formatting for transmission to a host computer.


ADDRESS BUS
BUS DRIVER
REFRESH
INSTRUCTION MEMORY
DISPLAY MEMORY
INTEL 8086 PROCESSOR
I/O PORT DECODE
LATCH
CLOCK
MUX
READ BUS
DATA BUS
DRIVER
WRITE BUS
COMPARE
I/O DRIVER
STATUS LATCH
CURSOR POSITION REGISTER
SERIAL INTERFACE
I/O BUS
INTERRUPT CONTROL
KEYBOARD
MODE CONTROL & INDICATORS
INTERACTIVE GRAPHICS

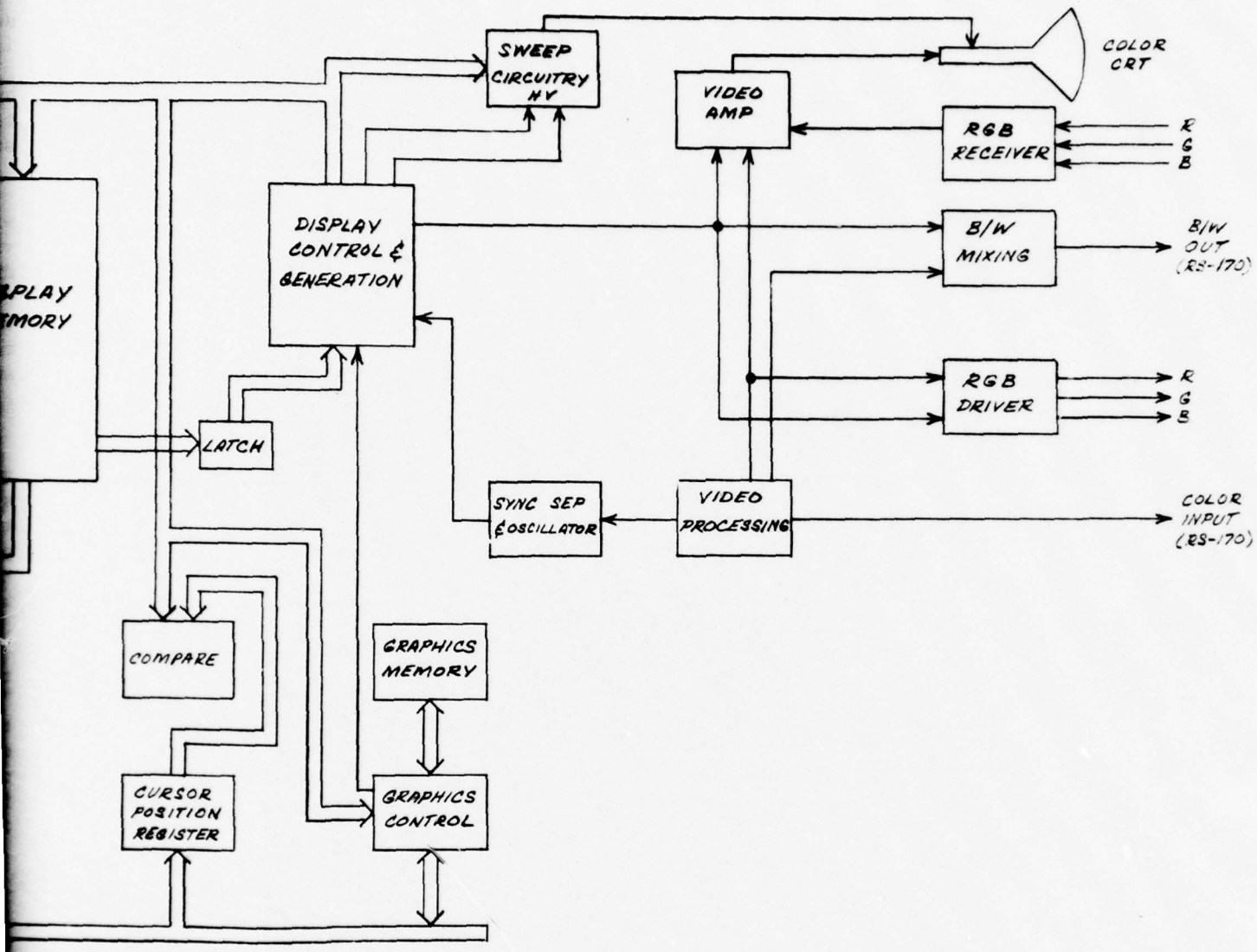


Figure 3.1 Controller Block Diagram

3.2 DISPLAY MEMORY

The display memory contains sufficient memory elements to store four pages of alphanumeric data or 7,680 characters (1,920 characters per page). Addressing is accomplished via the CP unit for data update or, in the normal refresh mode, from the display control and generator logic module.

Unique to color, 3 additional bits of information are added to each character storage position: 1 bit indicates a red character, 1 bit is for green, and 1 bit is for blue. A combination of red, green, and/or blue is then combined to generate the remaining four colors already identified for character display. These 3 bits, when read, control the gating action of the serial string of dot information to their respective video amplifier (R,G,B). This in turn controls the cathode voltage of the CRT, cutoff for a no-data bit to full saturation for the presence of a data bit.

3.3 DISPLAY CONTROL AND GENERATION LOGIC

This circuitry generates row and column counts that are used to address the refresh memory and position data properly on the screen. Because the character position is a direct representation of the beam position on the CRT, this addressing scheme is also made available to the sweep circuitry for addressing the convergence PROM used for the generation of correction currents to the convergence yoke.

This circuitry also generates horizontal and vertical sync pulses to the sweep circuitry thereby keeping the display in sync and jitter-free. Timing for this circuitry is provided by a delay line oscillator that is initiated in one of two ways. In the internal mode, the delay line is excited by a crystal oscillator running at 11.0236 MHz divided to 15,750 Hz. When connected to a video source, the 15,750 Hz sync pulses control the delay line causing the display data and composite video to be displayed in unison. Clocks available to perform shifting operations of displayed data operate at frequencies of 25 and 12.5 MHz generated as a result of the delay line oscillator.

3.4 GRAPHICS CONTROL AND MEMORY

Since this section of the controller is discussed in detail in Section 4 of this report, no further explanation will be made here.

3.5 VIDEO PROCESSING

The circuit description, previous studies, and approaches are discussed in detail in Section 5 and, therefore, will be omitted in this subparagraph.

3.6 VIDEO AMPLIFIER

The video amplifier requirements and operation discussion can be found in Section 6 of this report. Coverage of the retransmission circuitry and its capability will also be discussed later.

4.0 GRAPHICS

The character generation of the 1655 is done on a screen matrix of 640 dots by 480 lines. The graphic system for the 1655 uses this same matrix for graphic representation of red, blue, and green information. Each cell of the matrix is independently controlled with an intensity bit allowing either full or half intensity of the color indicated. A simple graphic system was necessary to minimize software overhead for the 8080 processor and keep the hardware implementation as inexpensive as possible.

4.1 MEMORY SYSTEM

The first consideration for the image memory was an implementation using the existing instruction memory cards. These cards are configured in four banks of 4K dynamic MOS memories (TI 4060 type) with an 8 bit word. The total capacity of these cards is 65,536 bits. To implement the 640 x 480 x 4 image memory would, therefore, require ten such cards. The power requirements for such a system are shown in Table 4.1.

One potential solution came with the announcement of the 16K RAMs. With a new memory card organized with five banks of 16K by 8 bits only two cards would be required. With the current vendor prices for the 16K RAMs, there is no savings in cost over the 4K RAM system, but the cost of the 16K RAMs is expected to drop significantly in the future. The power consumption of the 16K system is considerably better than the 4K (see Table 4.1). After investigating the physical and electrical impact of a system of this type, the availability of the 16K RAMs became a major problem. Delivery could not be guaranteed before 1/77 because of the vendor's production schedule. Because of the additional risk and impact to our development schedule, the 16K RAM system was rejected for this project, although it may be feasible for future systems.

One other developing technology for large memory systems is the Charge Coupled Device (CCD) memories. Within the past year three such devices have been made available: the Intel 2416, the Fairchild CCD 460, and the Fairchild CCD 450.

The CCD 450 is a serial storage memory consisting of 9,216 bits which are organized into a format of 1,024 bytes by 9 bits. This architecture is achieved with nine shift registers each 1,024 bits long. All nine registers are shifted in parallel so 9-bit bytes are stored or retrieved in a byte serial mode.

A block diagram for the device is shown in Figure 4.1. Each register is accessed by its own bidirectional data line, but all registers use common clocks and control logic. The memory can be easily expanded due to the tri-state TTL output stages. The device is available in a 1 MHz or 2 MHz version. To achieve data rates necessary for the display rate (80 nsec/bit), the device would have to operate at a speed of 1.38 MHz, which would require the high speed device. Operating at this speed, the worst case access time would be 738 μsec.

Table 4.1 RAM Current Requirements

VOLTAGE	WORST CASE CURRENT		TYPICAL CURRENT TOTAL
	PER CHIP	TOTAL SYSTEM	
+5	1 mA	1.28 A	1 A
+12	30 mA	37.6 A	10 A
-5	0.1 mA	128 mA	70 mA

A. 4K RAM Current Requirements

VOLTAGE	WORST CASE CURRENT		TYPICAL TOTAL CURRENT
	PER CHIP	TOTAL SYSTEM	
+5	5 mA	400 mA	100 mA
+12	35 mA	2.8 A	2 A
-5	200 μA	16 mA	10 mA

B. 16K RAM Current Requirements

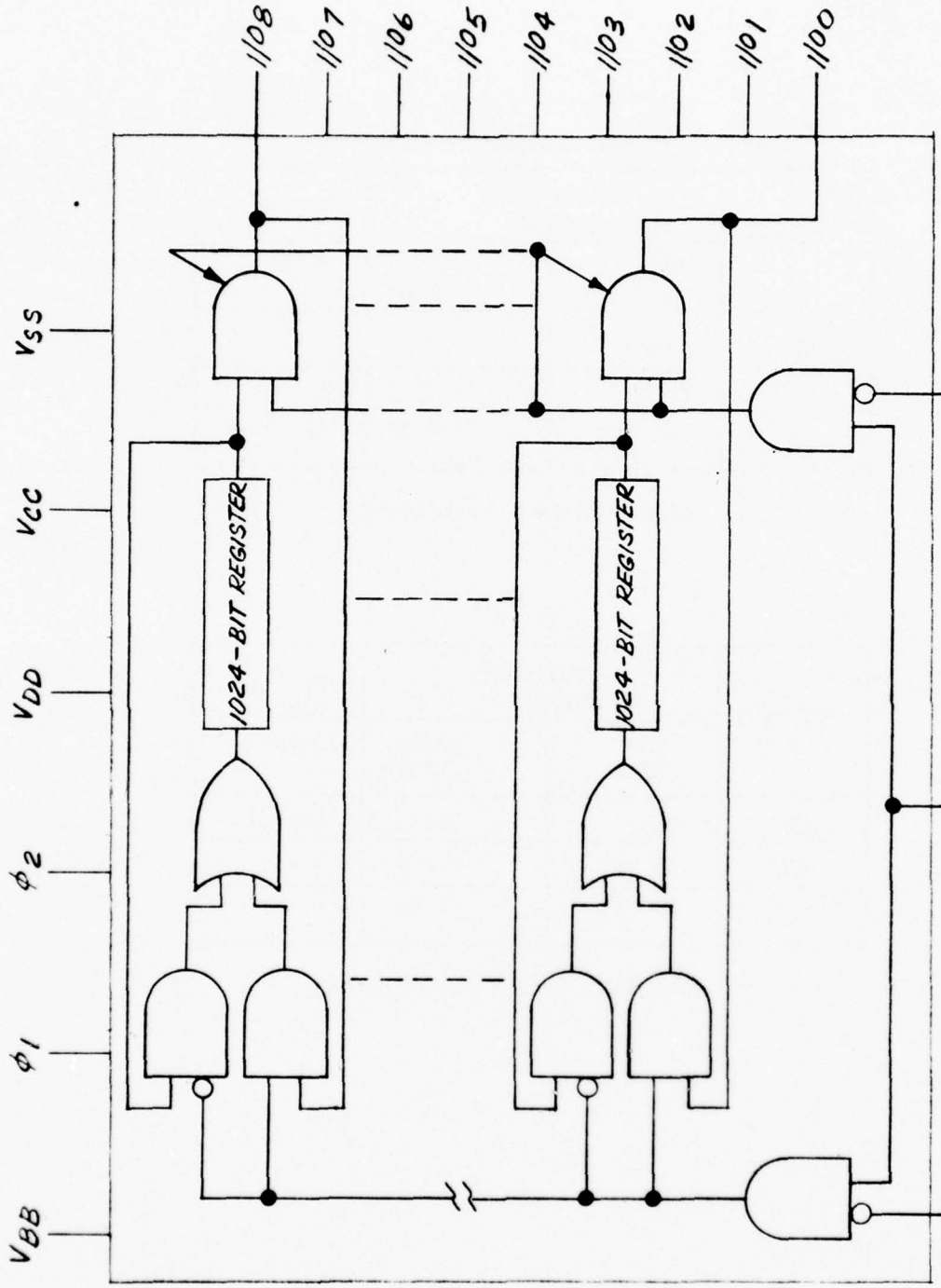


Figure 4.1 CCD Memory Block Diagram

To store the 307,200 bits for each color a minimum of 34 memories would be used. The worst case power for the CCD 450 is given by Fairchild to be 241 mw per chip. The power dissipated for the entire system could then be as high as 32.8 watts.

The Fairchild CCD 460 is a 16,384 dynamic Line Addressable RAM (LARAM). This device is organized as 32 addressable shift registers which are 128 bits long and 4 bits wide. Recirculation and shifting is automatic in the selected register. This organization is pictured in Figure 4.2.

In analyzing the latency time of these devices several considerations must be made. First, the maximum shift rate is 5 MHz. Secondly, while one register shifts, the others are stationary. And finally, screen refresh should not be interrupted while data is being sought. This means that the latency time could be as long as one entire shift cycle of the complete memory. This time can be determined by the shift rate of the system. For display purposes the data rate must be 80 nsec/bit. Since the 460 is a 4-bit parallel device, the shift rate would be 3.125 MHz. This yields a worst case access time of 1.31 msec.

A minimum of 76 CCD 460 memory chips would be required. The maximum power specified by Fairchild is 200 mw per chip. This would mean a worst case power dissipation of 15.2 watts.

The Intel 2416 is similar to the Fairchild CCD 460 in that it is a 16,384 bit LARAM. However, it differs from the Fairchild device in its organization. The 2416 is structured as 64 addressable shift registers of 256 bits each. The data in these registers is simultaneously shifted by exercising the four-phase clock signals. After a shift cycle, each of the 64 CCD registers can be selected for an input/output function by applying the appropriate 6-bit address code and applying chip enable, chip select, and write enable signals in the required manner. Figure 4.3 shows this organization.

To minimize latency times for processor read/write operations, the 2416 must operate with a shift-read-shift cycle. The minimum time for this shift/read cycle is 900 nsec. Since each memory is a single bit wide, at least 12 memories must be read in parallel to achieve the 80 nsec/bit display rate. But because 19 chips would be required for each of the R, G, B, and saturation memories, it would be simple to read all 19 chips in parallel. This would allow the shift read cycle to be as low as 1.6 μsec. With a cycle time of 1.6 μsec the worst case latency time would be 256 shift/read cycles or 410 μsec.

The maximum power specified by Intel for the 2416 is 300 nw. A system with the minimum memories (76) would therefore dissipate a worst case total of 22.8 watts. Investigation at Univac shows that the typical dissipation of the 2416 operating at 1.6 μsec is 160 mw. This would mean an expected typical dissipation of 1.44 watts.

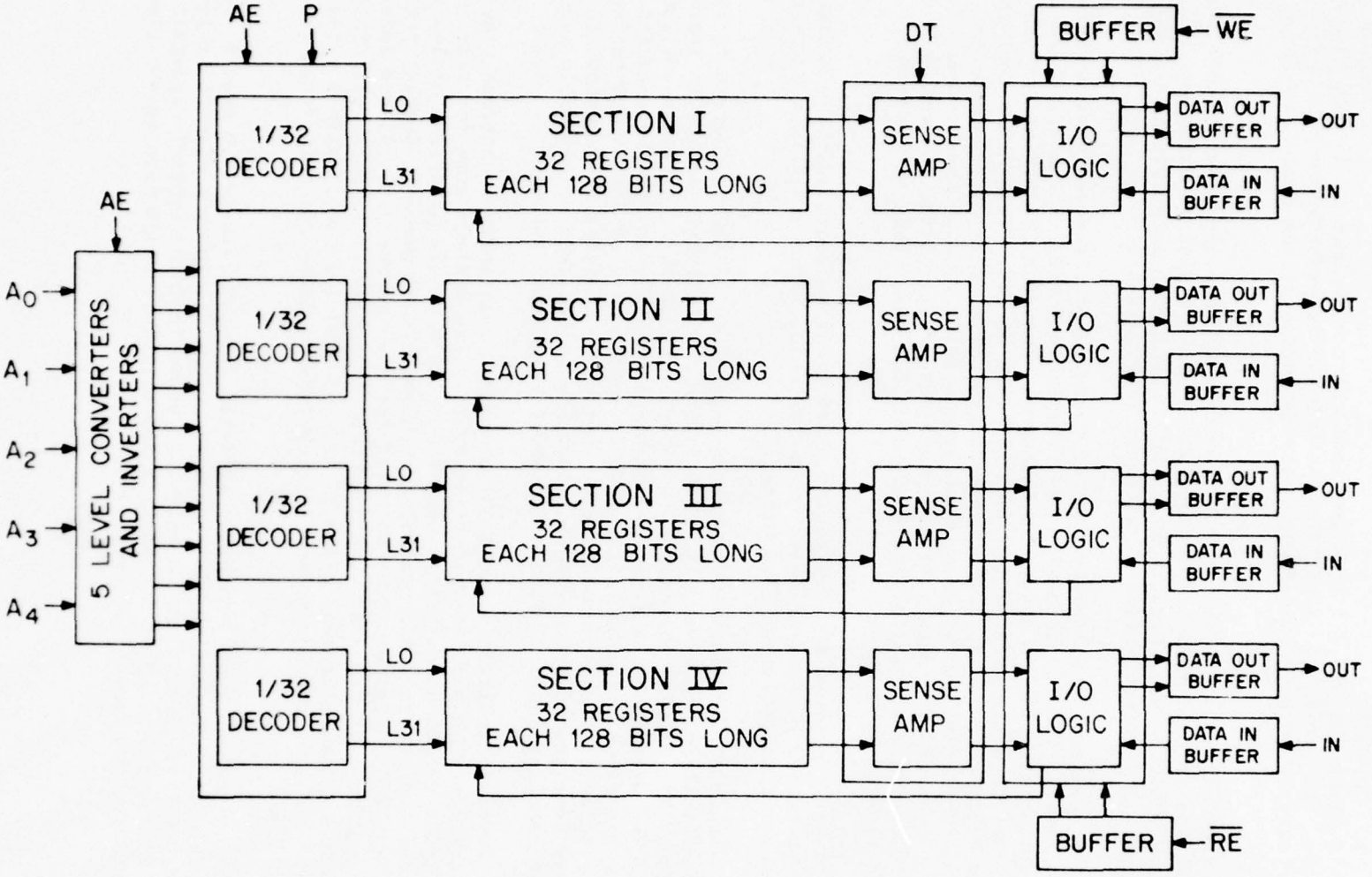


Figure 4.2 CCD Line Addressable RAM

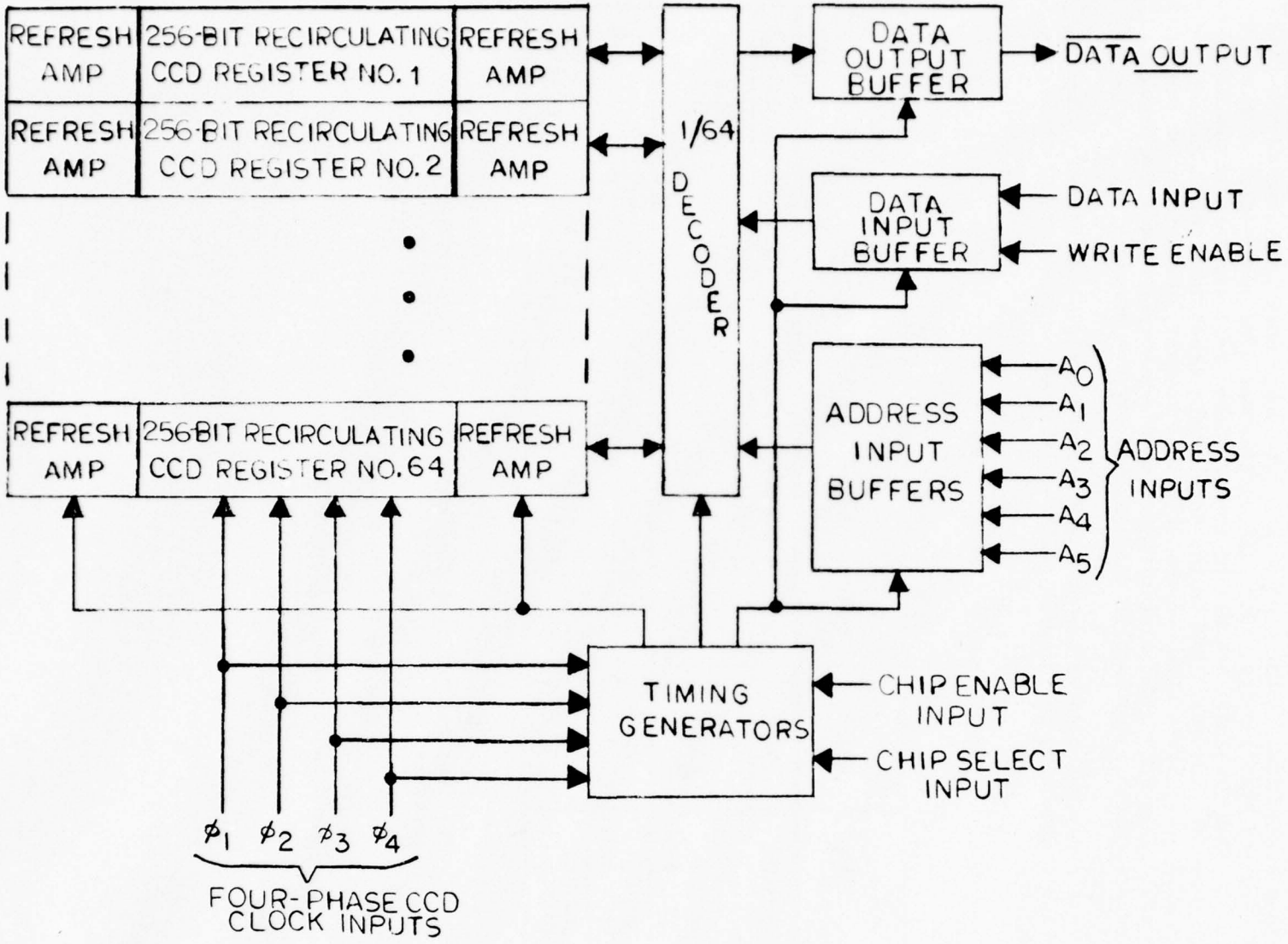


Figure 4.3 CCD LARAM

Table 4.2 is a comparison of each of the memories discussed showing the various trade-offs. After study, the 2416 looked most promising due to its low cost and high density. Its latency time was also much better than the other non-RAM systems. But due to the predicted delivery date it was felt that there was too much risk in the development schedule: the only parts available were the 4K RAMs and the 9K CCDs. However, the latency of the 9K CCD would have been a definite problem and the memory cost was too high; therefore, another approach to the image memory was sought.

A study was made to see if the memory size could be reduced without appreciably affecting the display quality. This would allow use of the 4K RAMs.

Table 4.2 Memory Comparison

MEMORY TYPE	MINN.[1] CHIPS REQ.	# OF BOARDS REQ.	POWER[2] DISS. TYPICAL	POWER DISS. WORST	WORST CASE LATENCY	AVAIL-ABILITY
4K RAM	300	10	120 W	216 W	0	9/76
16K RAM	76	2	12 W	32 W	0	1/77
9K CCD [CCD 450]	136	4	-	33 W	738 µS	9/76
16K CCD [CCD 460]	76	2	-	15 W	1.31 mS	?
16K CCD [2416]	76	2	2 W	22.8	410 µS	1/77

1. The data assumes that the most efficient architecture is possible.

$$N = 4 \times [307200 \div \text{capacity}] \text{ truncated}$$

2. The data represents experimental results observed at Univac.

The study determined that a smoothing scheme could be implemented with an image memory organized as 640 x 240. In this system the even lines would be displayed directly and the odd display lines would be generated using the smoothing algorithm. This would allow memory size, power, and cost to be reduced by 50% and only a small amount of circuitry required for the smoothing hardware. This would also allow the use of existing card types (Univac #7153506) in a 16K x 8 organization. All memory for the graphics system would reside on five of these card types. These findings convinced us to implement this approach.

The 7153506 memory card requires a one port memory that is multiplexed between display cycles and processor read/write operations. Because of the memory size (76,800 bytes) the system has to be independent of instruction memory and use a loadable X, Y address register for processor read/write cycles. The memory card can be wired in either an 8- or 16-bit configuration. An 8-bit byte orientation was chosen to simplify interface with the 8080 processor.

The 7153506 memory cards are organized in four banks of 4,096 8-bit bytes each. Since these are dynamic memories, a full refresh cycle must be completed every 1 ms. Because of this continuous reading, the memory for refresh display was designed to provide refresh through the normal display cycle. The architecture of the memory system is shown in Figure 4.4. Each of the 4 memory bits (red, blue, green, and sat) has been divided into five sections of 128 x 240. Each of these sections will be stored in one 4K x 8 bank of the memory. The design of the memory cards prevents the simultaneous reading of bank a and bank b or bank c and bank d. The architecture that is depicted prevents any memory conflicts from arising. It also allows the R, G, B, and saturation memories to be independent parallel memories. With this scheme the amount of memory wasted is minimized to about 6.5% (16 x 128 bits).

4.2 GRAPHIC CONTROL

The graphic control logic will allow three events to occur: display cycles, processor read cycles, or processor write cycles. These cycles will cause one 8-bit data word to be read or written into the graphics memory. Unless the processor has requested a read or write cycle, screen refresh will be accomplished via display cycles. A processor read or write cycle should require a minimum number of display cycles to be blanked. On even fields of the display frame the memory image should be displayed and on odd fields the dots generated by the smoothing scheme should be displayed.

A block diagram for the graphic system is shown in Figure 4.5, which depicts one of the four memories required in the system. Each of the memories consists of five 4K by 8-bit banks. The address for these memories is selected by the address MUX. The inputs to the MUX are the display address for screen refresh and the read/write address for processor operations. During display cycles the address MUX selects the display address. This address is generated partially by the Alphanumeric Display Control Logic (ADCL) and partially by the graphic control logic. The column count is used as generated by the ADCL but the normal row count generated is in modules of ten. The binary row count, therefore, must be generated by the graphic control logic.

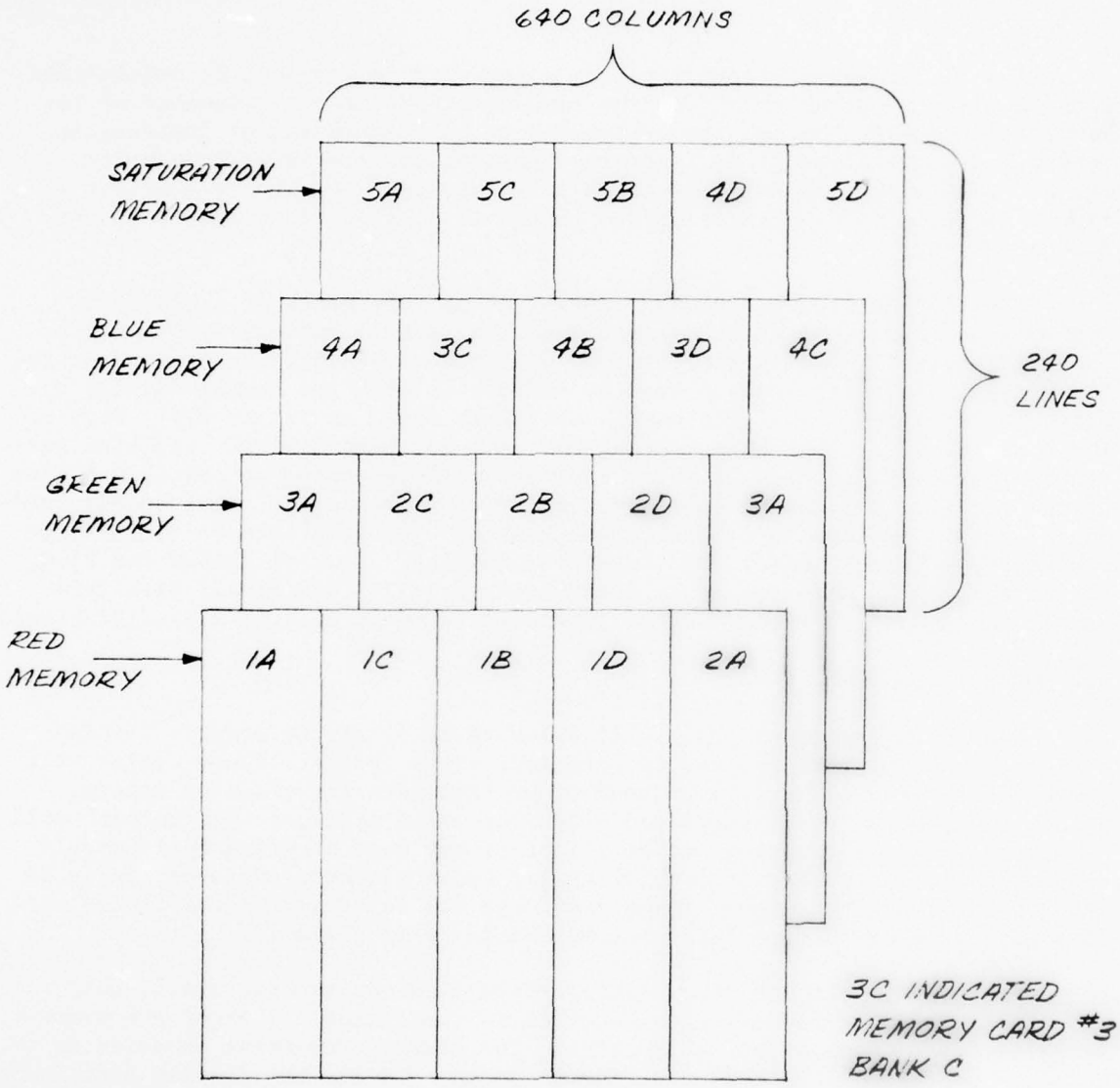


Figure 4.4 Memory Architecture

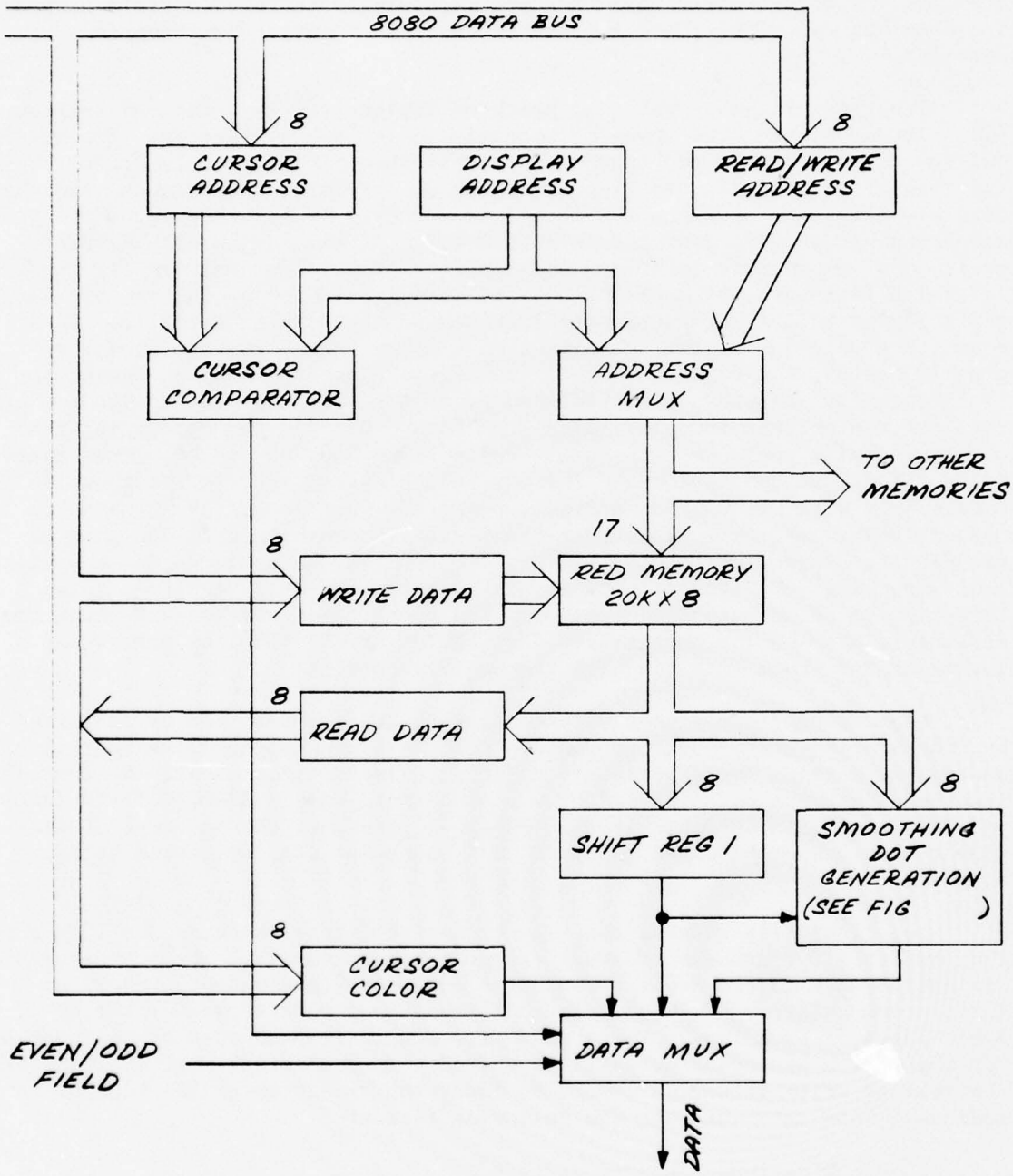


Figure 4.5 Graphic Control Block Diagram

When a display cycle is complete, the memory data is latched by the data shift register 1 and the smoothing dot generator. The shift register converts the 8-bit word to serial data at the display frequency of 80 nsec/bit. These bit serial outputs are then fed to the data MUX, which selects the shift register 1 output for even field display and the smoothing dots for odd field display. The data MUX can also select the cursor color if a cursor position is detected.

The smoothing approach that has been implemented is diagramed in Figure 4.6. It shows the three types of smoothing dots to be generated: the vertical smoothing dots and two types of diagonal smoothing dots. In order to make the transition from line to line as smooth as possible, the diagonal smoothing dots are generated at twice the normal frequency. The block diagram for the smoothing hardware is depicted in Figure 4.7. At the end of each display cycle, the memory data is loaded into shift register 1 as well as eight parallel shift registers, each of which is 80 bits long. The output of this long shift register is then exactly one line behind the data entering it. This means that when one of the 80 columns of display line N is read from the graph's memory, the same column of line N-1 is also available at the output of the long shift register. This delayed 8-bit word is then loaded into a shift register and shifted to delay flip-flops U1 and U2. At the same time, the output of shift register 1 is fed to delay flip-flops U3 and U4. From these delay flip-flops the conditions for the smoothing are decoded, as shown in Figure 4.7, with U1, U2, U3, and U4 sensing dot positions A, B, C, and D, respectively. AND gate G1 decodes the vertical smoothing dot; AND gate G2 decodes the diagonal smoothing dot, type 2; and AND gate G1 decodes the diagonal smoothing dot, type 1. The output of the decoder is sent to a delay flip-flop to be synchronized to the 25 MHz clock rate. Figure 4.8 shows the difference between the appearance of an arc on a full 480 line matrix and a matrix of 240 lines with the high frequency smoothing.

Each display cycle is always completed, but the next can be inhibited by processor intervention. Processor control is done through several input and output ports. These ports are defined in Table 4.3. Of all the control functions that can be initiated by the processor, only a READ INITIATE (output 24) or a WRITE INITIATE (output 20) will interrupt the sequence of display cycles. Each of these commands will cause two display cycles to be blanked.

The read/write address consists of two registers which can be loaded by the processor for processor access to the graphics memory. These registers are output port 23, an 8-bit row address ($0\text{-}239_{10}$), and output port 22, a 7-bit column address ($0\text{-}79_{10}$). The column address selects one of the 80 8-bit bytes of each line. This read/write address is selected by the address MUX whenever a processor access is required. The data that are received with the read or write request are used to increment or decrement the read/write address. This data word has the following format:

2^0 - H $\Rightarrow$ decrement column address

2^1 - H $\Rightarrow$ increment column address

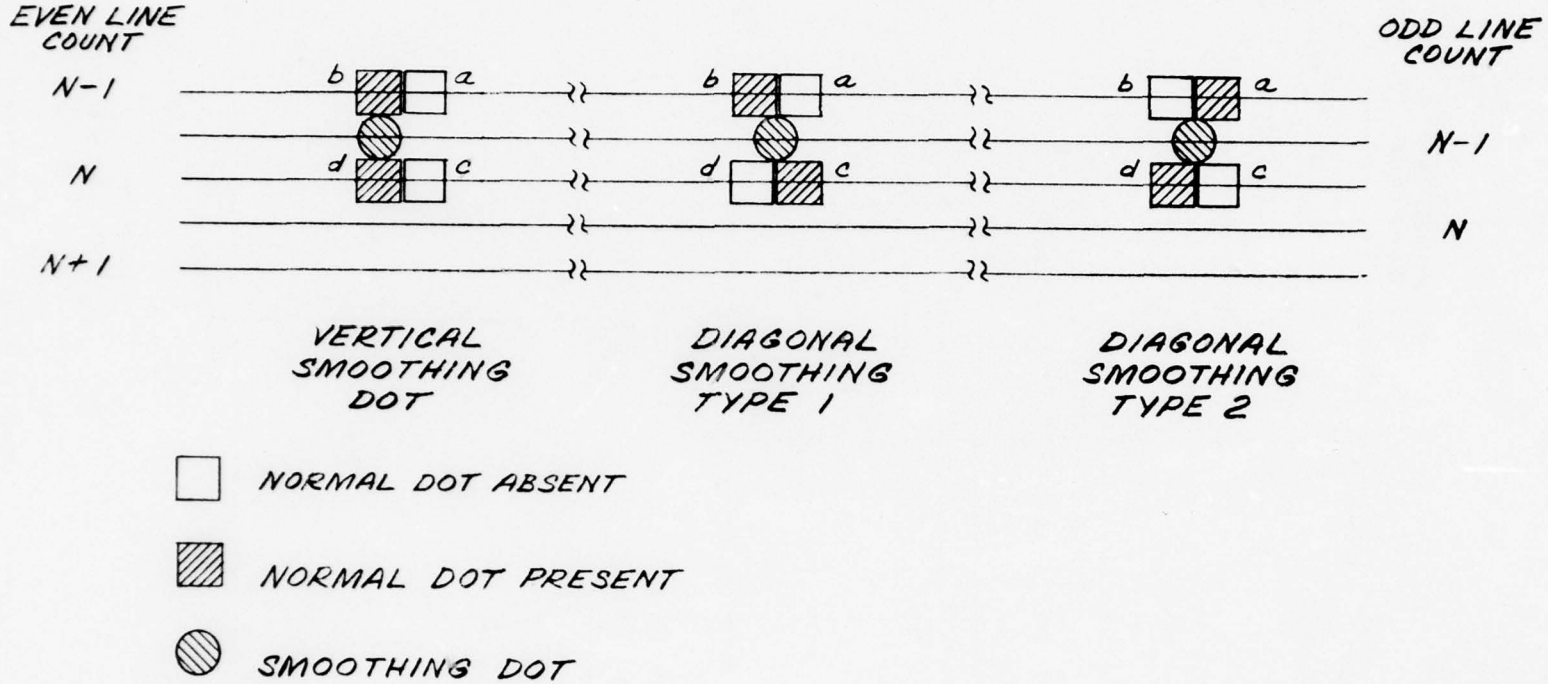


Figure 4.6 Graphic Smoothing Approach

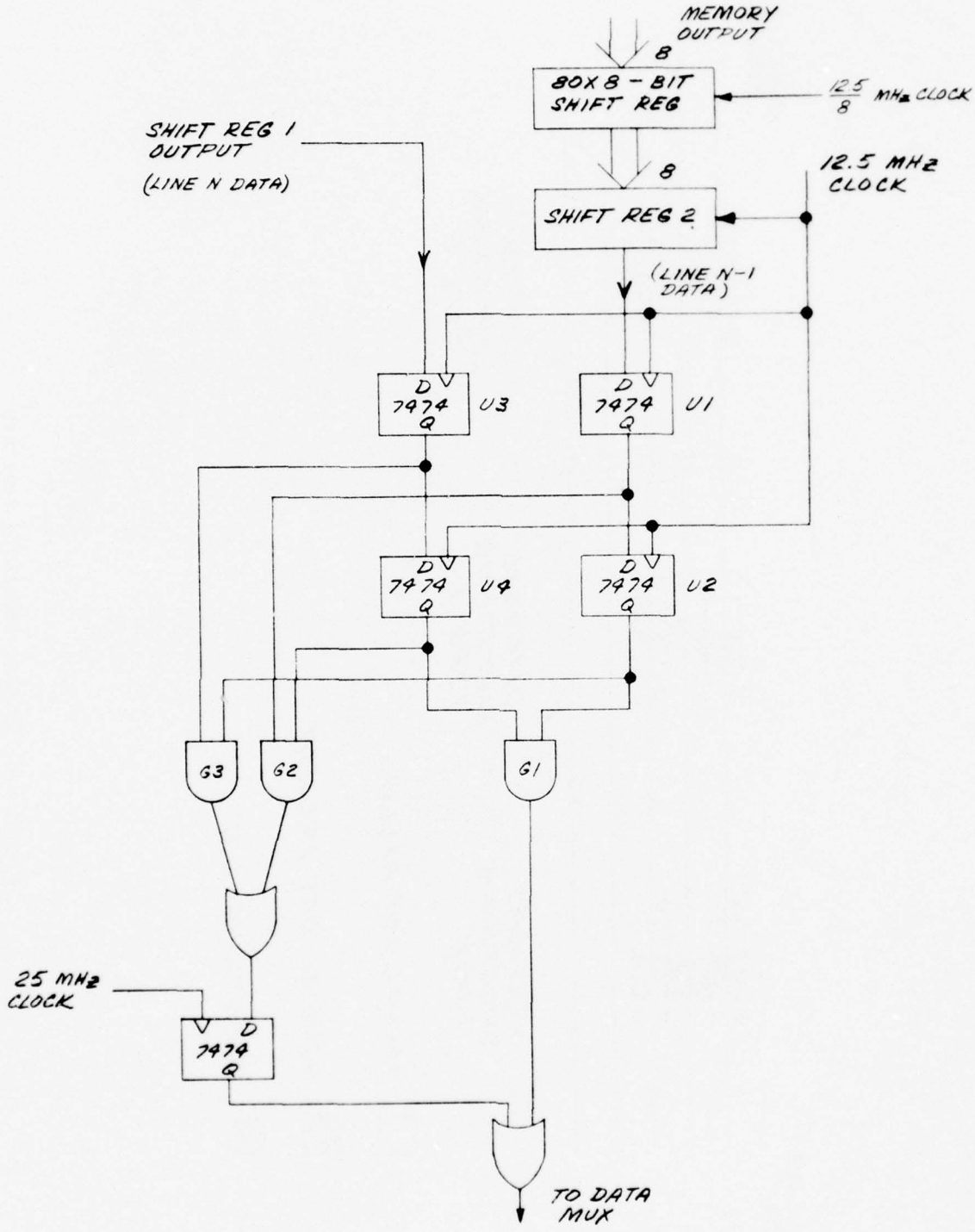


Figure 4.7 Graphic Smoothing Hardware

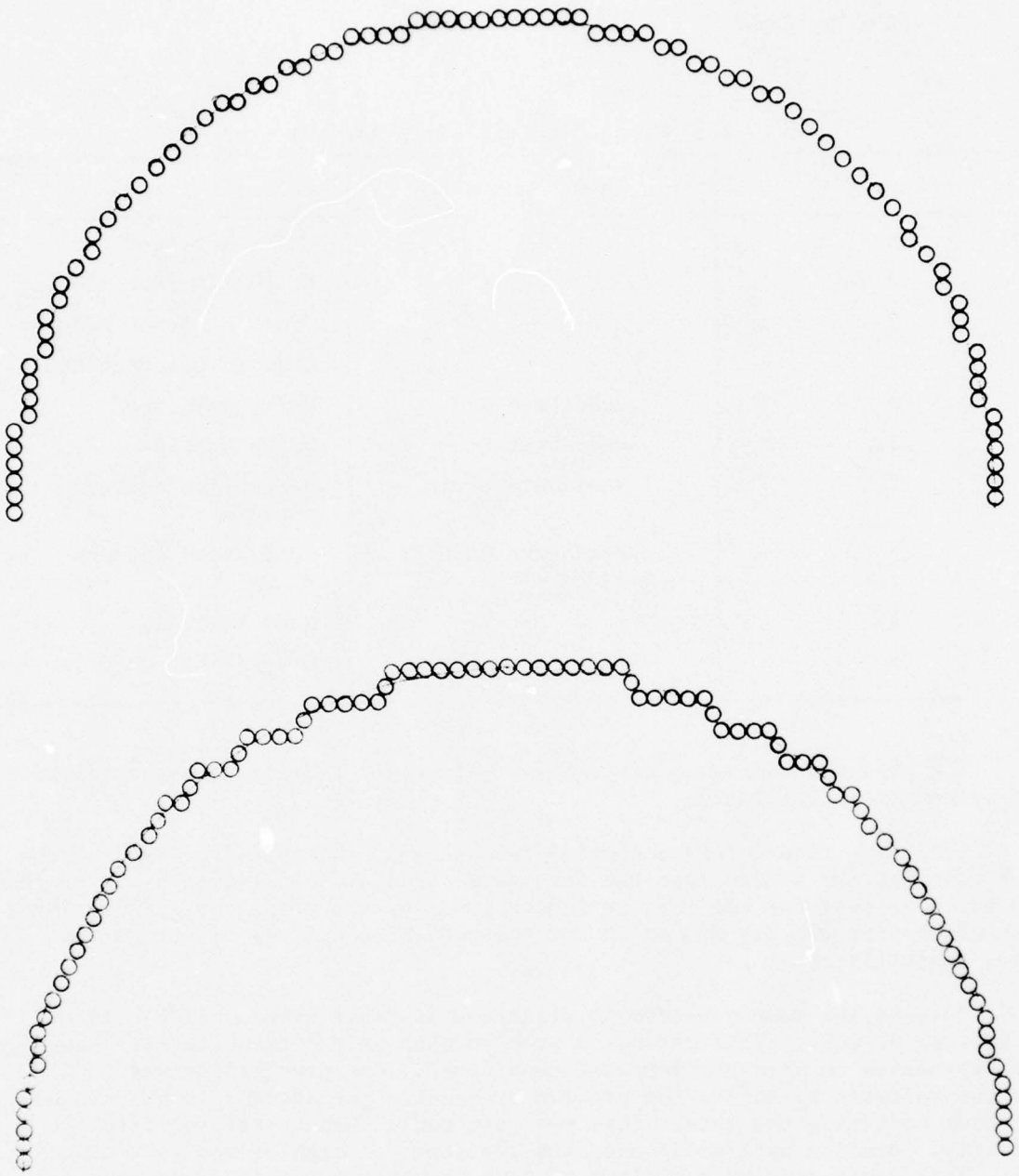


Figure 4.8 480/240 Matrix Comparison

2^2 - H ⇒ decrement row address

2^3 - H ⇒ increment row address

2^4 - 2^7 - Not used

Table 4.3 Graphic Control Port Assignments

Port #	Input Function	Output Function
6	-	Color Register
5	-	Graphic Cursor Address
7	-	Graphic Cursor Address
10	-	Graphic Cursor Address
20	Read Data Red	Write Initiate
21	Read Data Blue	Write Enable
22	Read Data Green	Read/Write Address (Column)
23	Read Data Saturation	Read/Write Address (Row)
24	-	Read Initiate
26	-	Graphic Cursor Color

The affected addresses are changed before the address is selected and the operation is initiated.

After the read initiate command is received, the data from each of the four memories are loaded into the read data register (see Figure 4.5) for that memory. The register can then be interrogated by the processor with an INPUT command on port 20, 21, 22, or 23 for the red, blue, green, or saturation data, respectively.

Because the memory system is organized as 8-bit bytes, all 8 bits must be written at once. This becomes a problem when only a few bits are changed. Two approaches to this problem were considered. One possibility was to allow the software to handle the problem by reading the address to be changed and then modifying the data. This new data could then be written into the specified location by loading one data register for each of the four memories. This would require a minimum of four input instruction executions and six output instruction executions as well as some data manipulation to calculate the new data word. The other approach would be to do this with the hardware by specifying which of the 8 bits should be changed and what color they should be. This would require only three output isntruction executions

and fewer calculations. As the writing speed of the system appeared more important than the additional hardware, the second approach was chosen.

Before a write cycle is initiated, the write data must be given. This is done by loading the desired color into the color register, port 6, which is also the color register for alphanumeric operations. This register has the following interpretation:

Color Register								Color
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
X	X	X	X	X	0	0	0	Black
X	X	X	X	X	0	0	1	Red
X	X	X	X	X	0	1	0	Blue
X	X	X	X	X	0	1	1	Magenta
X	X	X	X	X	1	0	0	Green
X	X	X	X	X	1	0	1	Yellow
X	X	X	X	X	1	1	0	Cyan
X	X	X	X	X	1	1	1	White
X	X	X	X	0	X	X	X	Full Intensity
X	X	X	X	1	X	X	X	Half Intensity

The other part of the write data is the write enable word which is loaded via port 21. This word is used to enable the write operation on any or all of the 8 bits of the word indicated by the read/write address. Each bit of this word that is set to logic zero prevents its associated bit in memory from being changed during the write operation. The following is an illustration of this operation:

Color = 0 0 0 0 0 1 0 1 (Magenta)

Write Enable = 1 0 1 1 0 0 1 0

Color Data before at read/write address before write operation.

Red Data = 0 0 1 1 0 1 0 1

Green Data = 1 0 0 1 1 0 0 1

Blue Data = 1 1 0 0 0 1 0 1

Saturation Data = 1 1 0 0 1 0 1 0

Color Data at read/write address after write operation.

Red Data = 1 0 1 1 0 1 1 1

Green Data = 0 0 0 0 1 0 0 1

Blue Data = 1 1 1 1 0 1 1 1

Saturation Data = 0 1 0 0 1 0 0 0

X X X X Bits unaffected by write

X X X X Bits written to magenta

The graphic cursor address register (see Figure 4.6) consists of output ports 5, 7, and 10. Port 5 is the cursor row address which has valid values of 0 to 239_{10}. The cursor column address is contained in ports 7 (LSB) and 10 (MSB). This address can be in the range of 0 to 639_{10}. This data is sent to the cursor comparator, which switches the data MUX to the cursor color when the display address corresponds to the cursor address. The cursor color is selected through an output to port 26 and has the same interpretation as the color register.

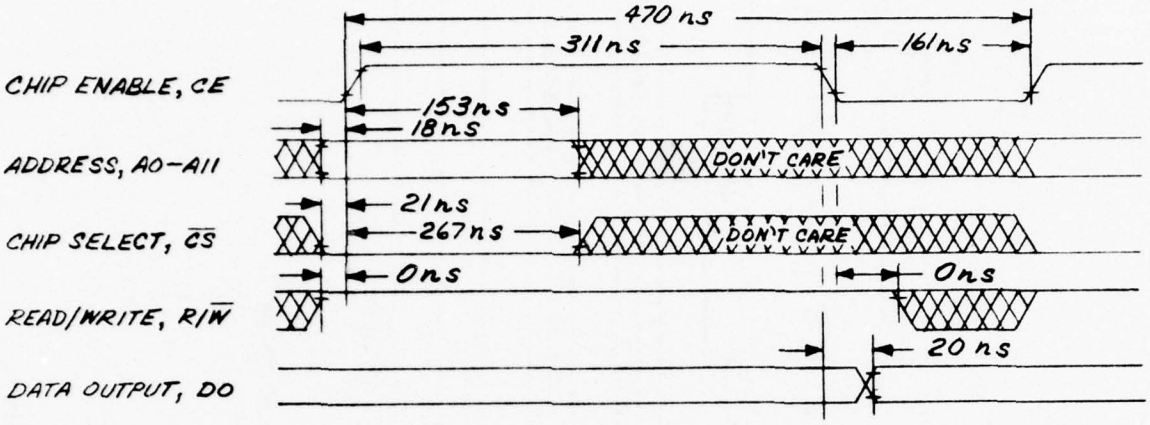
4.3 GRAPHICS TIMING

The timing requirements for the memory card are shown in Figure 4.9. These requirements, which have been defined by the Univac semiconductor engineering staff after studying the vendor-recommended timing and extensive testing of vendor parts, must be met to satisfy all approved vendors of the 4K RAM.

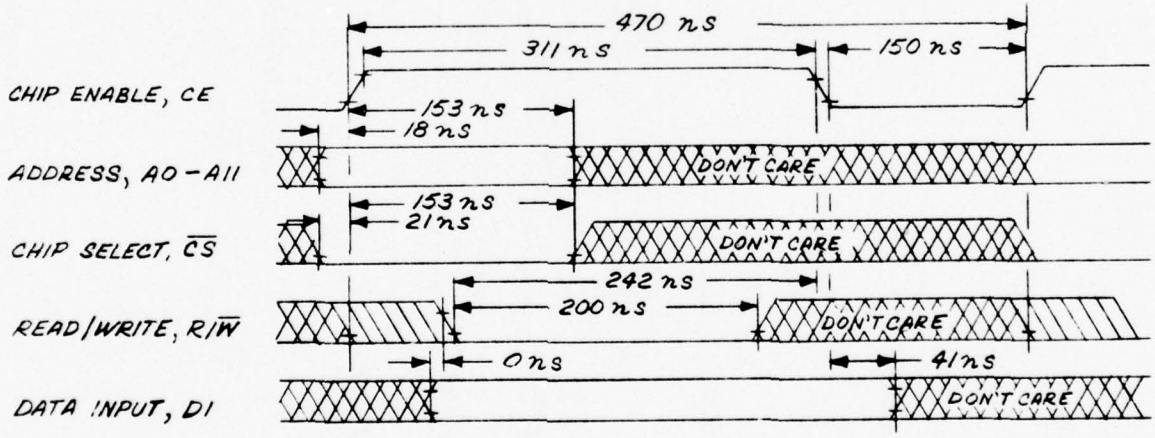
The timing for the graphic control logic is generated by the eight clock phases (ØA - ØH), the 12.5 MHz clock, and the 25 MHz clock. These signals are generated by the Alphanumeric Display Control Logic (ADCL). The display cycle timing is shown in Figure 4.10. The timing margin for each signal is shown on the figure. The display address is incremented on ØA, 350 nsec before the Chip Enable (CE) becomes active. The Chip Select (CS) signals are decoded from the display address lines and latched on ØE, which occurs 80 nsec prior to CE active signal. The data output is available 20 nsec after CE goes low (at ØC), so the 8 bit shift registers are loaded at ØD.

The write cycle timing is shown in Figure 4.11. The complete write cycle actually consists of one read cycle and one write cycle. This is necessary because writing can be inhibited on some or all of the 8 data bits of the data word. This is done under the control of the write enable word. Since the memory structure forces all 8 memory bits to be written at once, the original data must first be read and then rewritten into the bits which are write inhibited.

Both the read and the write occur at the read/write address that is selected by the data MUX. The data MUX is switched to ØD and the next CS is latched at ØE. This yields margins of 140 ns and 60 ns for the address and CS, respectively. During the write cycle the $R/\overline{W}$ is low for the entire CE active period, which means there are margins of 150 ns and 40 ns on the leading and trailing edges of the signal. The Data Output (DO) is available 20 ns after CE goes low at the end of the read cycle. These data are then gated with the write inhibit word and color register to develop the Data Input (DI) for the write cycle. The DI, therefore, has margins of 180 ns and 600 ns, as shown. The display blanking signal that is shown is used to inhibit the loading of the output shift registers.



MIN READ CYCLE TIMING



MIN WRITE CYCLE TIMING

Figure 4.9 Graphic Timing

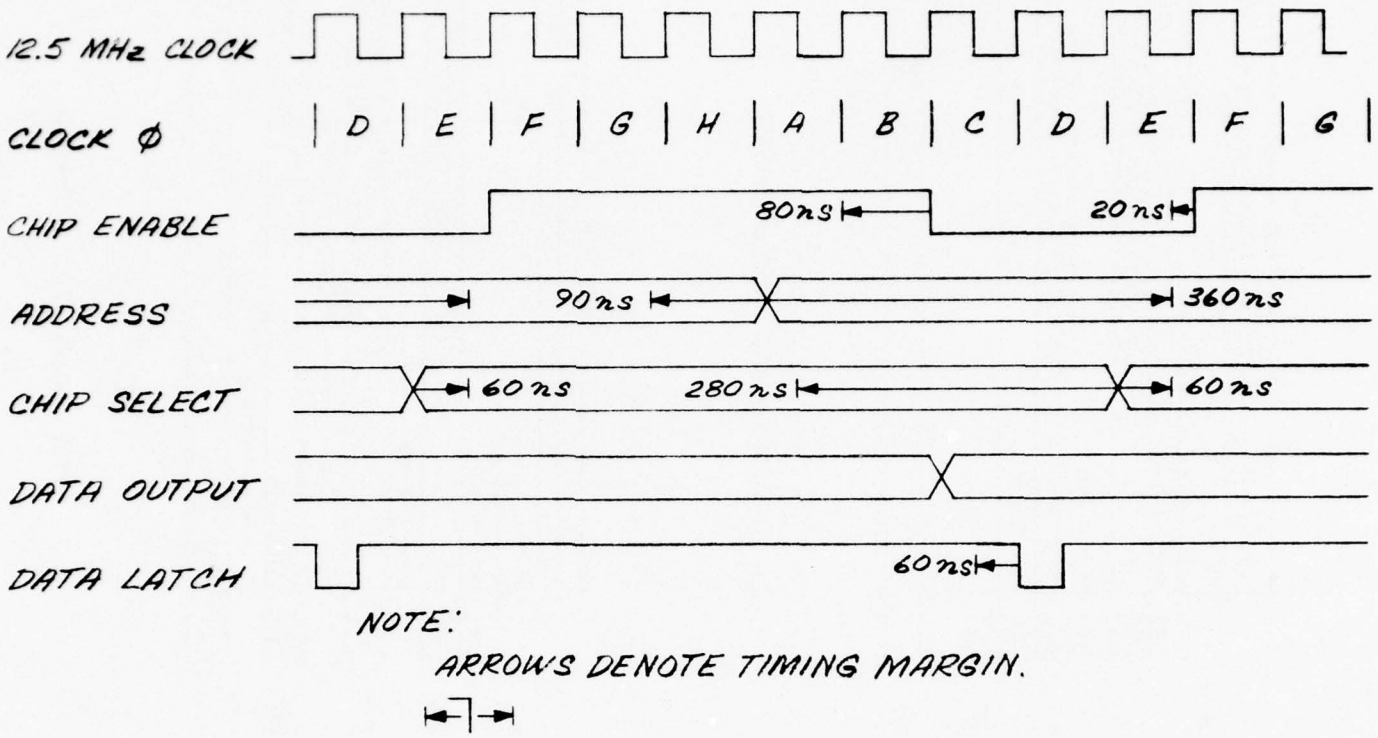
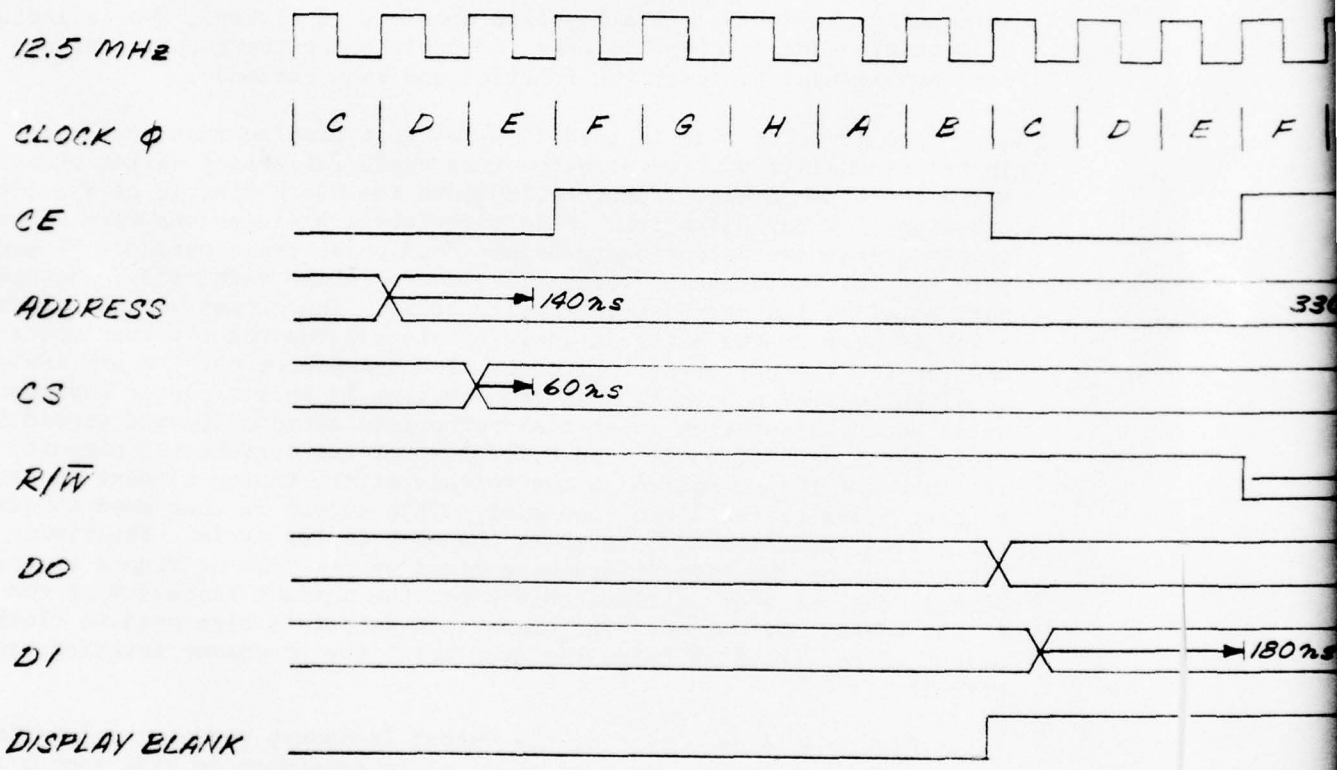
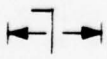


Figure 4.10 Graphic Display Cycle Timing



NOTE:

ARROWS DENOTE TIMING MARGIN.



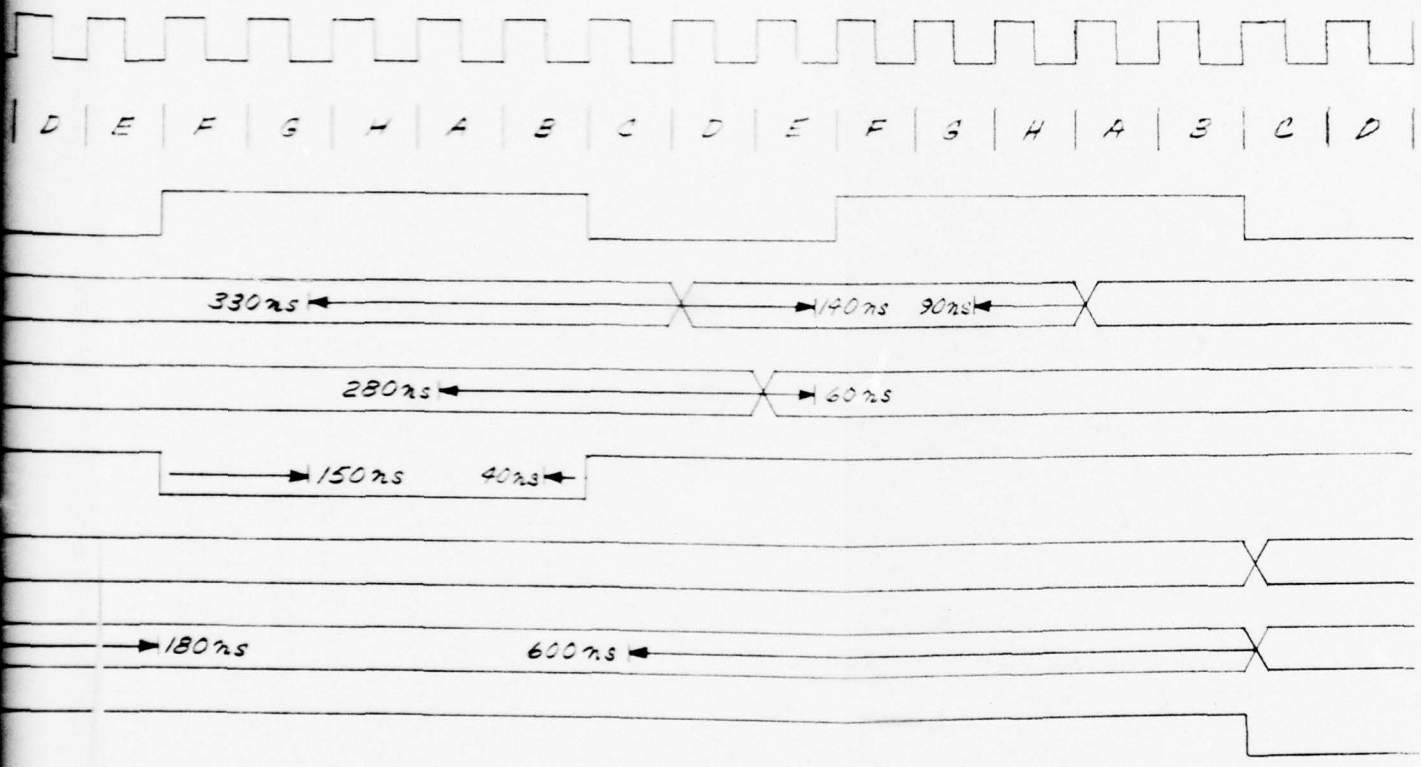


Figure 4.11 Write Cycle Timing

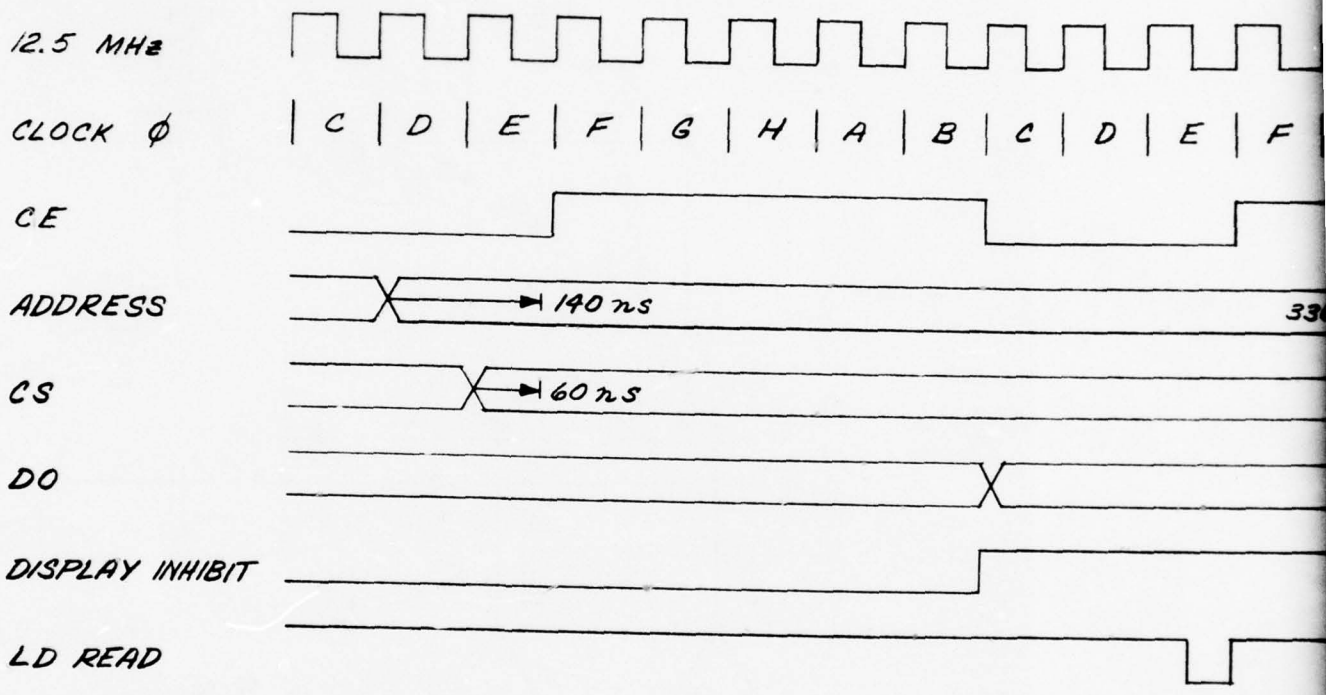
The read cycle timing is shown in Figure 4.12. This cycle actually takes two CE cycles to complete because of the time required to load the read data register. To minimize parts count, two 4 x 4 register files were used to store the four 8-bit data words. The timing for the read cycle is very similar to the write cycle. The address is switched at ØD and the CS is latched at ØE as before. The output data becomes available at the end off the first CE cycle and is loaded into the register file during the next cycle. Again the display is blanked for two display cycles.

4.4 INTERACTIVE GRAPHICS

The interactive graphic routines are controlled by the input from the interactive keyboard. This keyboard consists of 11 keys, two indicators, and a joystick. The joystick is used for positioning the graphic cursor, and the keyboard is used to input the function and type commands.

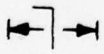
The joystick that is used is a low cost displacement type unit. This joystick consists of two potentiometers whose resistance varies proportionally to the stick angle. Figure 4.13 shows the block diagram of the interface circuitry for this joystick. This circuitry translates the varying resistances of the two potentiometers into four pulse train outputs. These outputs are for incrementing vertically, decrementing vertically, incrementing horizontally, and decrementing horizontally. The output voltage of the joystick is sent to two buffer/translator stages, one for the incremental circuit and one for the decremental circuit. The translator outputs are designed to be slightly over 6.2 volts when the joystick is in its center position and 0 volts when the joystick is at the appropriate extreme (toward ground for the decremental circuit and toward 6.2 volts for the incremental circuit). These voltages are then compared to the voltage at the timing element to generate a reset pulse to the 4 msec one shot. This output is then used to discharge the timing capacitor (C_T) to start the next timing cycle. The timing characteristics of the circuit are determined by the time constants R_T and C_T. Because the one shot is timed to 4 msec, the maximum frequency of the output is 250 pulses per second. The comparator output is also used to clock the output flip-flop which holds the data until the processor interrogates the circuit.

Figure 4.14 is a plot of the output frequency versus the joystick angle. The nonlinear nature of the plot is necessary to give adequate control at small angles but allow a high speed at the largest angles. It was felt that it would be necessary for the cursor to transverse the complete screen in under 3 seconds at the maximum speed. This means the maximum frequency would have to be at least 213 pulses per second. On the other extreme, the cursor must be able to move as slowly as one dot per second in order to have the required resolution. With a linear function these conditions cannot be met.



NOTE:

ARROWS DENOTE TIMING MARGIN.



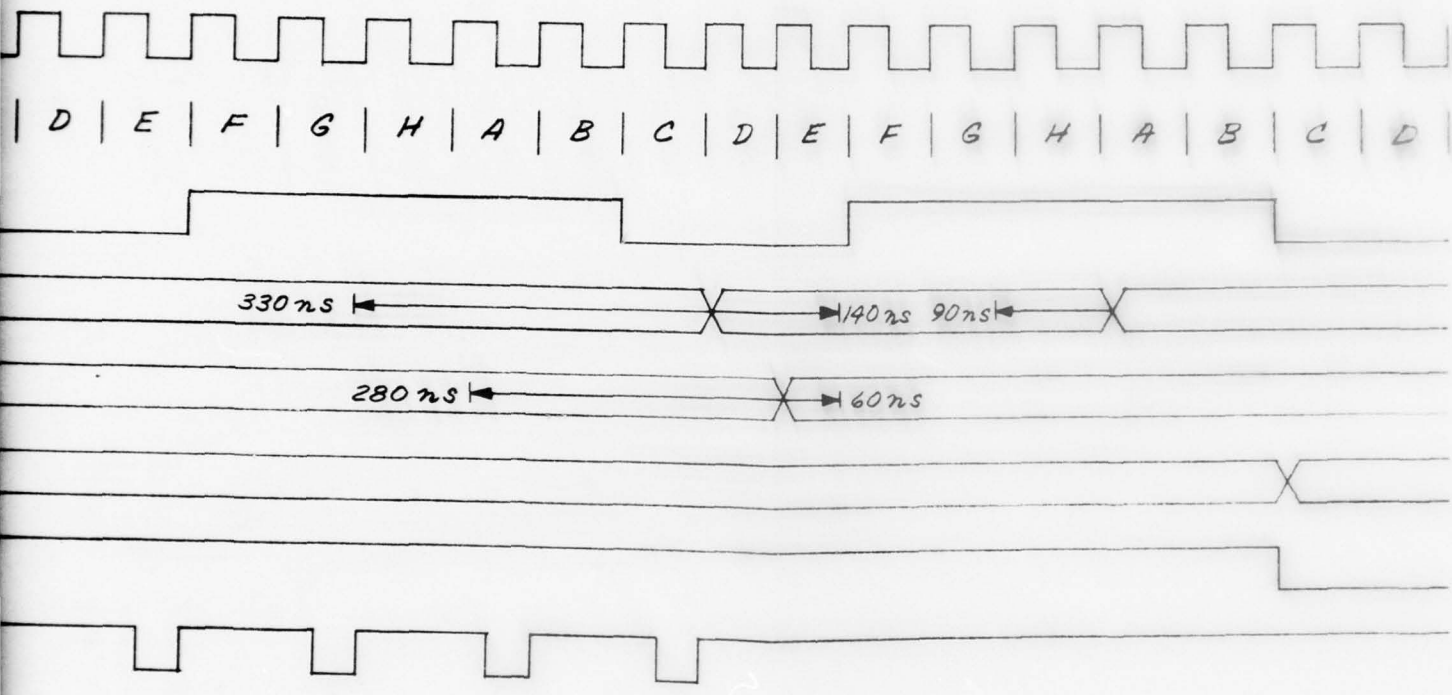
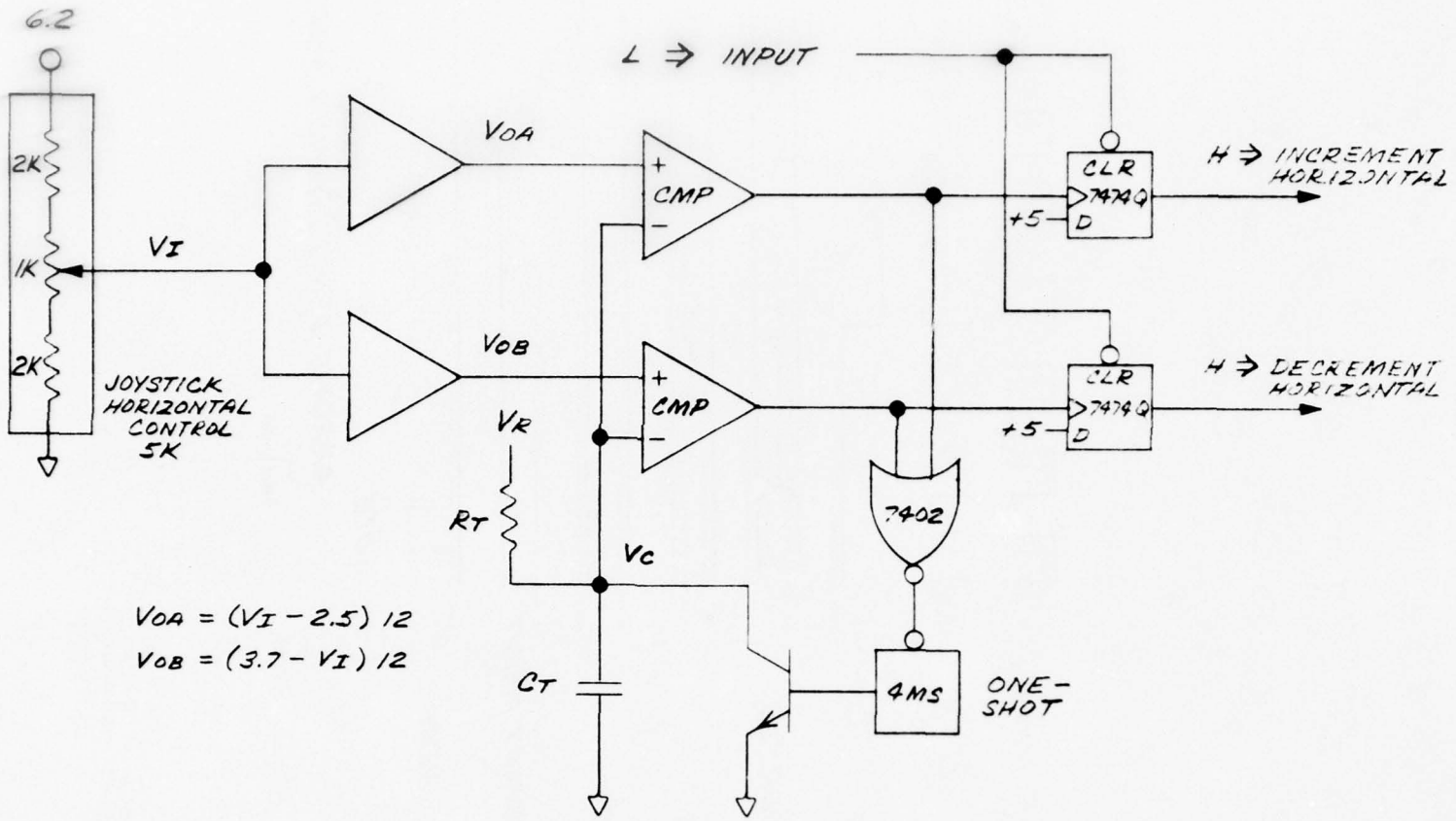


Figure 4.12 Read Cycle Timing

2



(Vertical circuit is same as horizontal circuit - horizontal circuit shown.)

Figure 4.13 Joystick Interface Block Diagram

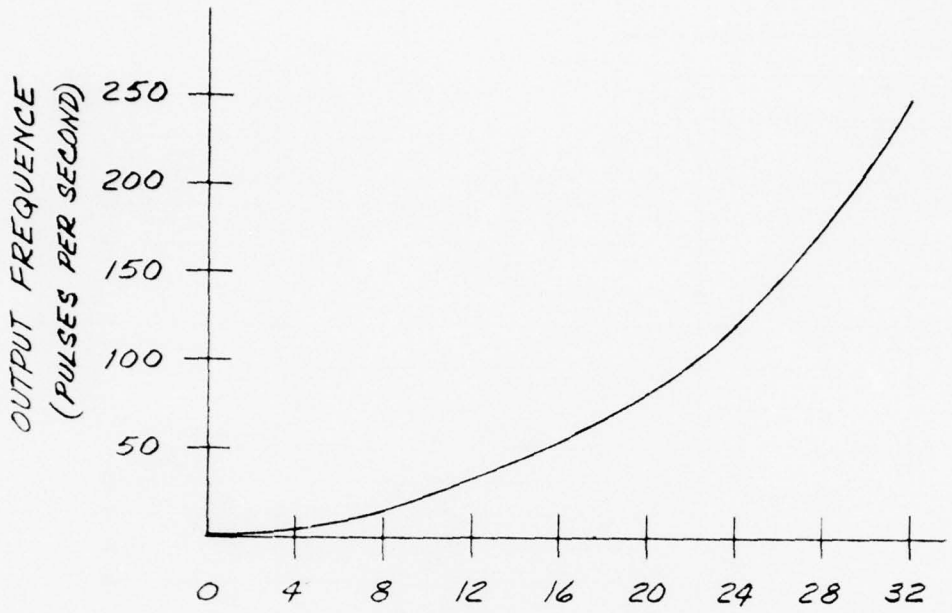


Figure 4.14 Joystick Angle

The interactive keyboard also contains 11 switches and two indicators. The circuitry required for these switches and indicators is diagramed in Figure 4.15. The switches are divided into two groups, the command switches and the function switches. These switches have the following interpretation:

GROUP 1 - Command Switches

Switch #1 - GENERATE
Switch #2 - BLINK
Switch #3 - RESTORE
Switch #4 - ERASE

GROUP 2 - Function Switches

Switch #5 - VECTOR
Switch #6 - VECTOR STRING
Switch #7 - ARC
Switch #8 - CIRCLE
Switch #9 - END STRING

When one of the switches is depressed, the switch inputs from that group are latched. These latched data are sent to the lamp drivers and the encoder circuit. The lamp drivers illuminate the switch which was depressed. The latches hold the data for the decoders, which in turn output to the data bus buffer.

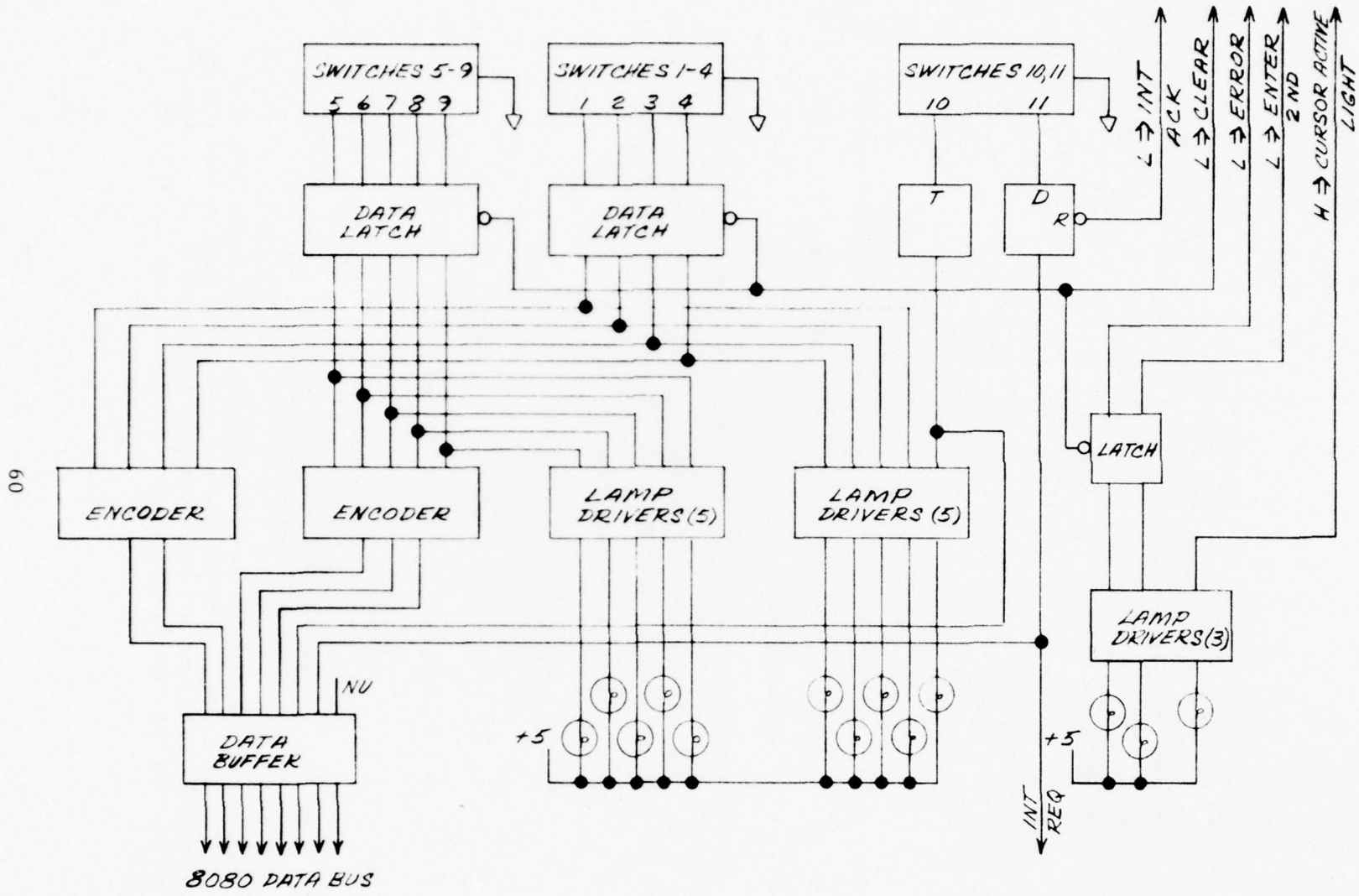


Figure 4.15 Interactive Graphic Keyboard

There are also two other switches on the keyboard. These are the CURSOR ACTIVE (CA) switch and the GRAPHIC MARK (GM) Switch. The Cursor Active (CA) switch is connected to a toggle flip-flop which changes state at each depression of the CA key. This action generates an interrupt request and sets a bit in the data word at the data bus buffer. The processor would then acknowledge the interrupt via an input instruction and either activate and deactivate the graphic cursor and then cause the CA key to be illuminated or to be extinguished.

The GM key is used to indicate to the processor that graphic parameters such as vector and points, circle center, circle radius, or vector string points are represented by the current position of the graphic cursor. With the depression of this key an interrupt is requested.

With each interrupt request, the processor must acknowledge it to reset the request flip-flop. This is done by interrogating the data word of the interactive graphic system. The processor interpretation for this word is shown in Table 4.4.

Table 4.4 Graphic Data Word Interpretation

Data Word								Processor Interpretation	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^1		
0	X	X	X	X	X	X	X	Cursor Not Active	
1	X	X	X	X	X	X	X	Cursor Active	
X	X	X	0	0	0	X	X	Illegal Code	Command Codes
X	X	X	0	0	1	X	X	Vector	
X	X	X	0	1	0	X	X	Vector String	
X	X	X	0	1	1	X	X	Circle	
X	X	X	1	0	0	X	X	Arc	
X	X	X	1	0	1	X	X	End of String	
X	X	X	X	X	X	0	0	Restore	Function Codes
X	X	X	X	X	X	0	1	Blink	
X	X	X	X	X	X	1	0	Erase	
X	X	X	X	X	X	1	1	Generate	

The two indicators on the interactive keyboard are the error light and the enter second light. These lights are illuminated under processor command via an output instruction. The error light indicates that the processor cannot complete the instructions that have been entered. For example, an operator positions the graphic cursor on a vector string then depressing BLINK,

VECTOR, MARK. Because the item at the cursor is not a vector, the error indicator illuminates the corrective action is awaited. The enter second light is illuminated whenever further data is expected. For example, an operator generates a circle, positions the graphic cursor at the center of the desired circle, and then depresses GENERATE, CIRCLE, MARK. The first depression of the mark key indicates that the center point of the circle has been entered. The processor should respond by illuminating the enter second light to indicate that the first data has been accepted and that more data is needed. These lamps are lit by the processor through an output to the interactive graphic control word. This word has the format specified below:

2^7 - H ⇒ Cursor Active Light On

2^6 - NU

2^5 - H ⇒ Clear Graphics Memory

2^4 - H ⇒ Enable Graphic Cursor

2^3 - NU

2^2 - H ⇒ Error Light On

2^1 - H ⇒ Clear All Indicators

2^0 - H ⇒ Enter Second Light On

5.0 VIDEO INPUTS

The video input for the 1655 can be in one of two forms. Included are provisions for a high bandwidth RGB system with a separate line for synchronizing the signal and also a conventional RS-170 video input. This RS-170 standard input may be either color or black and white, but is limited to a lower frequency response than the RGB system.

The RGB system requires four interconnections for its use: the Red video (R), Green video (G), Blue video (B), and the Synchronizing (SYNC) signal. The SYNC signal is received by a comparator, which compares the input voltage to a fixed reference. The TTL output of this comparator is then fed to the sync separator to develop the vertical and horizontal sync signals.

The RS-170 system requires a single interconnection for reception from an external source. This interconnection has all the information necessary to reproduce a color or black and white video picture. The synchronizing must be a part of the received signal, in accordance with RS-170 standards. The color information, when present, is phase encoded onto the analog video information at a frequency of 3.58 MHz. This phase encoding technique limits the bandwidth to 2.5 MHz because of the side bands generated by the phase changes of the 3.58 MHz signal. The phase and frequency of the color subcarrier is transmitted with an eight-cycle burst of a reference signal on the back porch of the horizontal sync pulse. The demodulation of the phase encoded subcarrier signal can be done with several commercially available integrated circuit chip sets manufactured by several companies. To choose one of these systems, Univac conducted an evaluation of the available demodulators.

Two or three integrated circuits are required for processing of the color video signal from the camera. The number of circuits depends on which system is used. Tests were performed on two Motorola, one Fairchild, one National, and one RCA processing systems.

The first system tested used a Motorola MC1398P integrated circuit for the 3.58 MHz subcarrier generation and chroma amplifier and a Motorola MC 1324P integrated circuit, with luminance input, for the color demodulator.

Subcarrier regeneration by the MC1398P circuit is, as was the case for all the circuits tested, accomplished by synchronizing a crystal oscillator with the color burst signal. A gate pulse that is developed at horizontal retrace time enables the oscillator driver in the MC1398P to synchronize with the color burst signal, which is on the back porch of each horizontal sync pulse. The color burst pulse, along with the chroma information, are amplified by the chroma amplifier and then gated to the oscillator.

The amplified chroma signal along with the 3.58 MHz subcarrier is applied to the MC1324P color demodulator. For demodulation of the chroma signal two 3.58 MHz frequencies with a phase shift of 90° between them is necessary. Therefore, a phase shift circuit of discrete components was necessary for all the color demodulator circuits tested. The MC1224P demodulator has the capability to add the luminance signal to the R-Y, G-Y, and B-Y signals that

were generated in the demodulator. This addition produces R, G, and B signals, which can be applied to the Univac-designed final amplifier driving the CRT.

Component layout was important for all the circuits tested. Using the vendor-suggested application and layout, the MC1398P subcarrier generator was rather unstable. A small amount of stray capacitance, such as an oscillscope probe or a person's hand, brought close to the crystal oscillator circuit would pull it off frequency. After consultation with the vendor it was learned that new subcarrier segments and color demodulator circuits had been developed. These circuits were tested, and the results are noted later in this report. Because of the inability of this circuit, no further testing of the MC1324P and the MC1398P was done at this time.

The National system requires three integrated circuits to do the color processing. An LM3071 is used for the chroma amplifier, an LM3070 for subcarrier regeneration, and an LM746 for the color demodulator.

The LM3071 chroma amplifier has two stages of amplification. The gain of the first stage is controlled by the automatic chroma control detector, and the gain of the second stage is controlled by the chroma gain control. Output from the first stage is applied to the LM3070 subcarrier regenerator along with the horizontal gate pulse to sync the 3.58 MHz subcarrier oscillator. Color demodulation is done in the LM746, which uses the 3.58 MHz subcarrier and the output from the second stage of the chroma amplifier to generate the R-Y, G-Y, and B-Y signals.

This system does not provide a way to add the luminance signal to the R-Y, G-Y, and B-Y signals. The final amplifiers that drive the CRT must combine the luminance and chrominance signals. Design of the final amplifier for the TX600B monitor does not have this capability. For this reason, and because a rather large number of discrete components was used in addition to the integrated circuits, there was no further development of the National system.

Commercial television receiver printed circuit modules built by RCA were also tested. This system uses two modules. One module has a CA3066 integrated circuit for the chroma amplifier and subcarrier regeneration. The other module uses a CA3067 integrated circuit for the color demodulator. Output from the subcarrier oscillator in the CA3066 was stable, with an amplitude of 2 volts peak to peak. This was the greatest amplitude of any of the systems tested. A horizontal gate pulse is required to sync the 3.58 MHz oscillator. Color signals from the demodulator were also stable and clean. As with the National system, the RCA system produces R-Y, G-Y, and B-Y color signals. The final amplifier must add the luminance and chrominance signals. It was stated before that the Univac design for the final amplifier does not do this. For this reason no further development was done on the RCA system.

Fairchild uses a UA787 integrated circuit for the chroma amplifier and subcarrier regeneration and a UA788 integrated circuit, with luminance input, for the color demodulator. The component layout and grounding were found to be very critical to all systems. Fairchild furnished a printed circuit board with the component layout. This simplified the development and tuning of the

system. Design of the UA787 circuit does not require an adjustment for the automatic color control or the color killer threshold. However, it does require a horizontal gate pulse to sync the 3.58 MHz oscillator.

The 3.58 MHz subcarrier and chroma signal were applied to the UA788 color demodulator integrated circuit. These signals together with the luminance input produced R, G, and B color signals that could be applied directly to the Univac final amplifier. The system is compatible with the TX600B monitor and was satisfactory.

Motorola introduced a system which uses an XC1399P integrated circuit that is the same as the other circuits that have been discussed. Input signals it requires are the chroma signal, which includes the color built signal, and the horizontal burst gate pulse, which allows the color burst to synchronize the 3.58 MHz crystal controlled oscillator. Adjustments for automatic phasing, automatic chroma control, and color killer threshold are included in this system.

The phasing control shifts the 3.58 MHz oscillator frequency to exactly the same phase as the color burst frequency. Gain of the chroma amplifier is adjusted by the chroma control to maintain correct chrominance amplitude in relation to the luminance amplitude. When receiving a monochrome transmission it is necessary to disable the chroma amplifier to make sure there is no color on the screen. To do this, the killer threshold control is adjusted to detect the color burst signal. During a monochrome transmission, no color burst is transmitted. If there is no color burst detected, the chroma amplifier is disabled.

The demodulator used in this system is the MC1323P integrated circuit. It requires the chroma signal and the subcarrier, generated by the XC1399P, for demodulation. With the capability to add chrominance and luminance signals, the output from the MC1323P are R, G, and B signals and can be applied to the Univac designed final amplifier. The operator was stable with satisfactory output levels. This system is currently installed in the demonstration monitor with good results.

A review of the color processing circuits shows that all subcarrier regeneration circuits have voltage regulators incorporated in them. With an input of 24 volts DC applied, the regulator output was around 12 volts DC. The regulator improves the stability of the 3.58 MHz (exact frequency, 3,579,454 MHz) oscillator. All systems require a crystal to control the oscillator and a horizontal gate pulse to allow the burst pulses to synchronize the oscillator. The output amplitude of the oscillator is 1 volt peak to peak except for the RCA system, which is 2 volts peak to peak.

All demodulator circuits require a tint control to adjust the shade of color and a color control to adjust the color brightness. The Fairchild μA788 and the Motorola XC1399X demodulators are capable of adding the luminance and chrominance signals. A DC component that is established by the brightness of the scene that is transmitted must be maintained through the demodulator and final amplifier. Therefore, circuits to match the luminance input signal to

the demodulator and the R, G, and B outputs to the final amplifier are necessary. The luminance input bias level to the XC1399 is 2 volts and 16 volts to the μA788. R, G, and B output bias levels are about 2 volts for the Motorola XC1399 and Fairchild μA788 demodulators. R-Y, G-Y, and B-Y demodulator output bias levels are 10 volts for the National LM3071 and 4 volts for the RCA module. Video gain from input of the chrome amplifier to the demodulator output is 50 for the Motorola system, 40 for the National system, 10 for the RCA system, and 4 for the Fairchild system.

With a 2 volt bias level at the luminance input and a gain of 50 for the system, it was decided to install the Motorola XC1399 and MC1323 circuits in the demonstration monitor.

With each of the color demodulators described some preprocessing of the received video signal was required. This preprocessing included line termination and buffering, signal amplification, subcarrier extraction, subcarrier suppression in the luminance signal, sync signal stripping, and burst gate generation. There are two integrated circuits which handle at least one of the above functions and have been tested by Univac. These circuits are the Motorola MC1344 and the Matsushita AN249.

The Motorola MC1344 integrated circuit contains a sync separator, a noise inverter, and an automatic gain control for the RF and IF stages. In the MC1344, only the sync separator is needed. Using the vendor-recommended circuit for testing the sync separator, it was found that the sync output was very sensitive to changes in the video input amplitude. The sync output was compatible with our system, but because of the poor stability and the excess circuitry contained in the chip, other systems were investigated.

The Matsushita AN249 integrated circuit includes a sync separator and video amplifier. The sync output was compatible with our system and has good stability with input variations from .5 volts to 1 volt. The video amplifier has a gain of seven but the amplifier exhibited some nonlinear characteristics. There exists no second source for this part. The AN249 was used for some time until further investigation could be completed.

Because of the problems mentioned with each of the preprocessing chips, a Univac design effort was begun. The block diagram for the final design of this system is shown in Figure 5.1. The video input is terminated to 75 ohms as required by RS-170 and it is then capacitively coupled into the summing amplifier and peak detector. The peak detector generates a positive voltage equal to the amplitude of the negative peaks of the video input. The positive voltage is then added to the video with the summing amplifier, as shown. The output of this amplifier is, therefore, a positive voltage with the sync signal going to ground. The output of this stage is used as the chroma input for the color demodulator and also as the input for the subcarrier trap. This trap is a band stop filter tuned to 3.58 MHz, which is 3 db down at 2.6 MHz and 4.6 MHz. The filter output is then used to develop the composite sync output and luminance signal. The signal at this point still has the sync pulses at ground. However, the input to the control and delayed video output needs to be black level at ground. To accomplish this level shift, the level of the backporch is sampled and used as a correction voltage for the DC

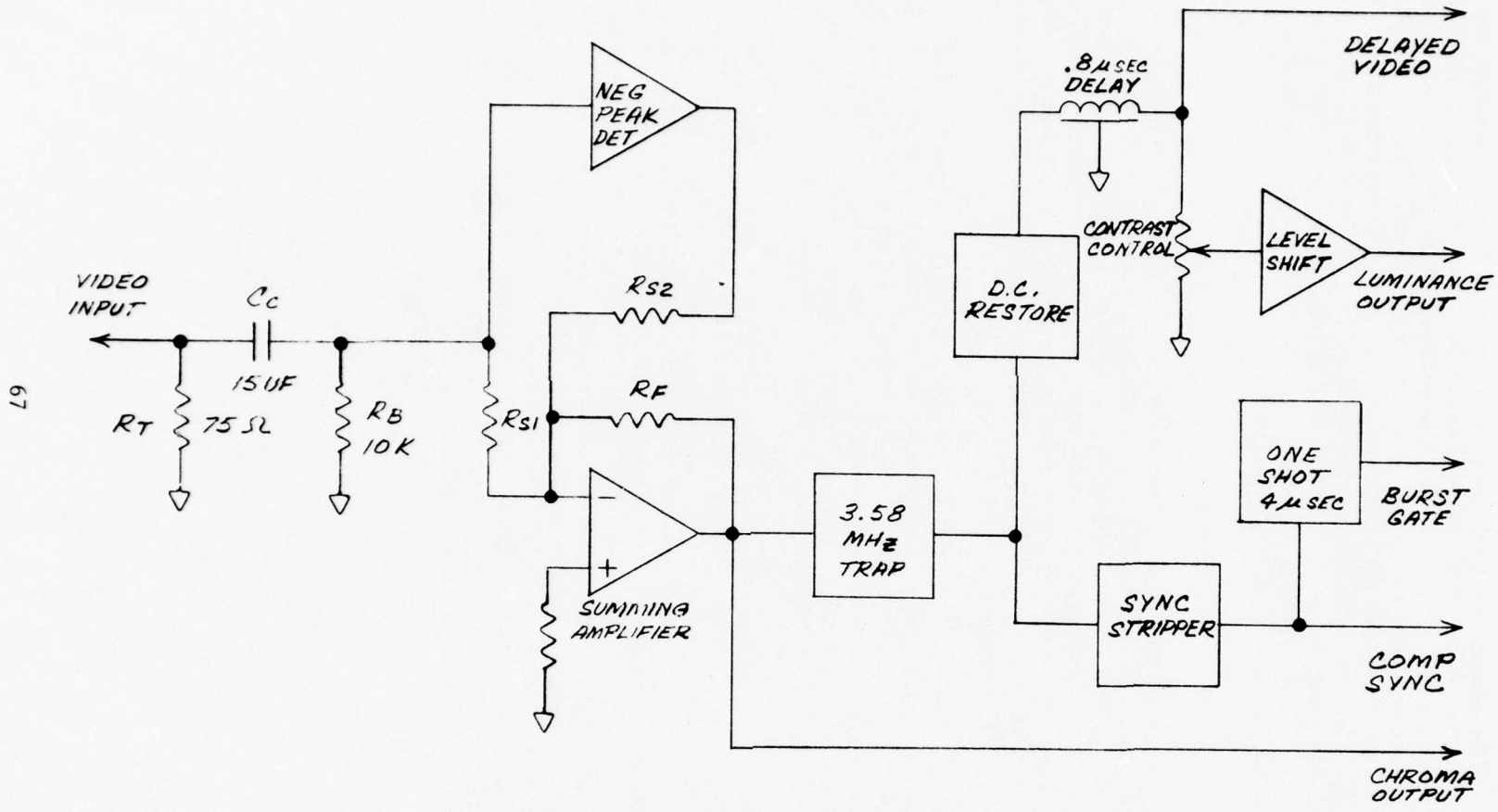


Figure 5.1 Luminance Amplifier

restorer. This output is then delayed by about .8 μsec o match the delay of the color demodulator. The delay line output is then sent to the black and white retransmission circuitry via the delayed video signal and the contrast control, as shown. The output of the constrast control is inputted to the level shift to match the DC requirements of the luminance input of the color demodulator. In the demodulator these signals (chrome, burst gate, and luminance) are used to generate the red, green, and blue components of the video signal. These output signals are then sent to the video amplifier to be amplified and applied to the CRT cathode.

5.1 VIDEO OUTPUTS

The video output that is generated by the 1655 is available in two forms. forms. One is an R, G, B, and SYNC system compatible with the RGB input. These outputs are a 1 volt, black negative signal capable of driving 75 ohm lines. The video signals are taken from the video amplifier output at the CRT cathode. These transmitters are briefly described in Section 6. The SYNC signal output is also a 1 volt sync negative signal which has timing in accordance with RS-170 composite sync.

The other retransmission system is made for integration into a black and white video system. This output combines the luminance signal of the video input with the digital information (character and graphics) to develop a true RS-170 composite output. The colors of the characters and graphic information are transmitted as white data with half the intensity area produced as grey. The black diagram for the system is shown in Figure 5.2.

The delayed video input contains all the luminance information from the video input. Gain block K4 then amplifies and shifts the video information to the specification of RS-170. This signal is then ORed with the digital inputs. These digital inputs are the full or half intensity display information and the sync signal. Gain block K1 is used to develop the proper voltages, as defined in the RS-170 specification for the synchronizing signal. Gain blocks K2 and K3 are used to superimpose the half and full intensity digital information. This digital information is an OR of the R, G, and B digital signals, as shown. These inputs have both character and graphic information represented in them. K2 has the gain required to drive the output to full intensity when enabled and K3 has the gain required to drive the output to half intensity when enabled.

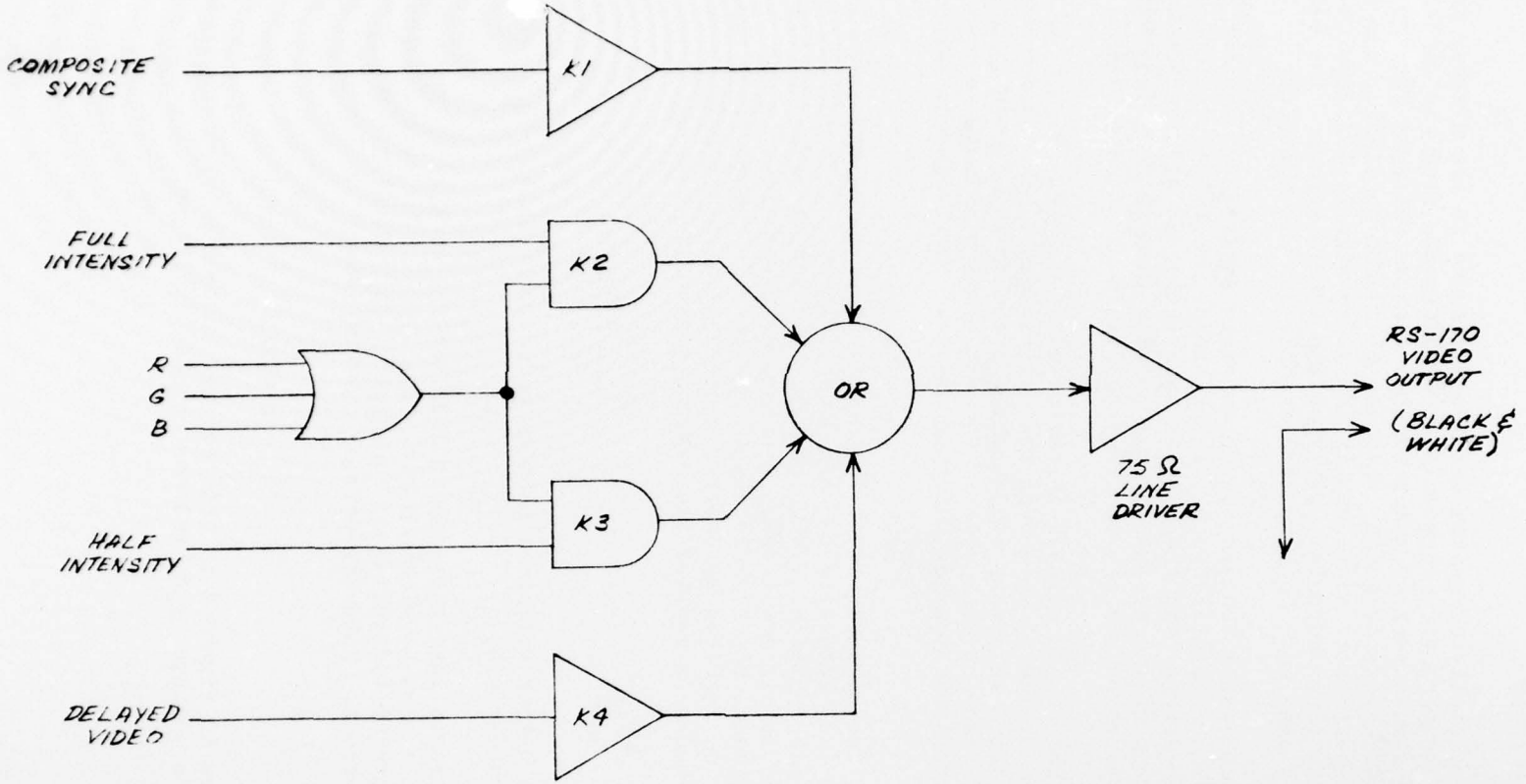


Figure 5.2 Monochrome Retransmission Block Diagram

6.0 VIDEO AMPLIFIER

The video amplifier system developed for use in the display combines signals from a camera via a demodulator with signals from the control logic (graphics and alphanumerics) and generates cathode voltages for the color CRT. The system must have a frequency response of 17 MHz to display the characters and graphics sharply and must amplify the video signals linearly to preserve intensity variations and color purity of the camera signal. The saturation of the graphic data must be modulated at half or full intensity.

The video system contains three separate amplifiers, one for each gun, which mix video and digital data for each color, together with common control amplifiers for determining the graphic saturation and video intensity. Figure 6.1 is a diagram of the system for one color. This is repeated three times, with the exception of the common elements within the dashed lines.

The mixing of the signals is performed by summing, at a node, currents representative of the video and of the digital data. The summed current is then used to drive an output stage, which produces the cathode voltage to drive the CRT beam for each color. Current summing is done to avoid voltage swings and capacitive loading and thus preserve the frequency response of the system.

The CRT cathodes require a voltage swing of +5 to +40 volts to modulate the beam from full intensity to zero, respectively. This voltage is developed by a common-base amplifier, which converts the sum of video and digital currents into the required voltage. A common-base amplifier is used to avoid Miller capacitance, which would negate the fast (20 nsec) risetimes required. The amplifier Q_1 requires an emitter current given by Equation 1 to fully drive the cathodes on and for the present system is about 52 ma.

$$I_E = \frac{40 - V_{BIAS}}{R_C} \tag{6}$$

Note that the output voltage cannot go below approximately V_{BIAS} due to an antisaturation diode D_1.

The currents into the summing node are the emitter current and a current consisting of a bias level minus the video level. The currents leaving the node are a current indicative of the digital data (full or half saturation) and a bias current. Thus the emitter current from Q_1 is given by Equation 2.

$$I_E = I_{DIGITAL} + I_{VIDEO} \tag{7}$$

As can be seen in Figure 6.1, this emitter current is then converted linearly into a cathode voltage by Q_1 and the cathode amplifier.

The digital input receives logic level signals from the display control logic indicative of whether the cathode should be off or on at that particular position of the raster. These signals switch transistor Q_2 to either saturation or cutoff. Thus the summing node is switched to a voltage determined by the output of the saturation amplifier at the emitter of Q_3. Simultaneously with any digital data (either alphanumeric or graphic) the video is disabled so that I_{VIDEO} is zero. Then the emitter current of Q_1, given in Equation 3, is only determined by the digital current.

$$I_E = \frac{V_{BIAS} - V_{VEQ1} - V_{EQ3}}{RE} \tag{8}$$

Thus, this current and hence the cathode voltage, half or full saturation, can be varied by a suitable choice of V_{EQ3}, which is determined by the saturation amplifier.

The saturation amplifier is common to all three amplifiers and receives a logic level signal from the display control logic indicative of whether the digital graphic data displayed at that particular raster position should be either half or fully saturated. The amplifier develops a voltage which drives the emitter of Q_3 on each color amplifier to either of two levels. The lower voltage level forces a maximum emitter current of about 52 ma, as depicted by Equation 3. The higher or half saturation voltage forces an emitter current of about 26 ma. This drives the cathode voltage to about 22 volts, which causes a half intensity beam in the CRT. The exact voltage is adjustable by a common level control to set the desired half intensity beam level of the CRT. The half saturation command is only enabled during graphic information where it is used to shade in graphics areas, such as circles and squares.

The video current is generated in response to video signals R, G, and B received from the demodulator. The three separate color outputs from the demodulator are about +6 volts at full intensity and decrease to about +4 volts at no intensity. The demodulator signal is applied to the video amplifier portion of the video system. (Refer to Figure 6.1.) The amplifier has separate gain and level adjustments. It rejects the level upon which the actual color signal is impressed. The output is indicative of only the signal portion of the input and can be adjusted by the gain control independently of the level.

The video is enabled only when there is no graphic or alphanumeric information to be displayed. This is done to preserve the color purity and saturation of the digital data. The video is turned off so that a black hole is created into which the desired graphic or alphanumeric data is put.

The video is enabled via a common video brightness amplifier shown in Figure 6.1. This amplifier receives a logic signal from the display control logic and changes the emitter voltage of Q_4 to one of two levels. When the video is enabled, the voltage can be adjusted by a level control and is nominally 16 volts. Disabling the video raises this voltage to about 17 volts. This voltage and the output of the video amplifier determine the current entering the summing node from the collector of Q_5.

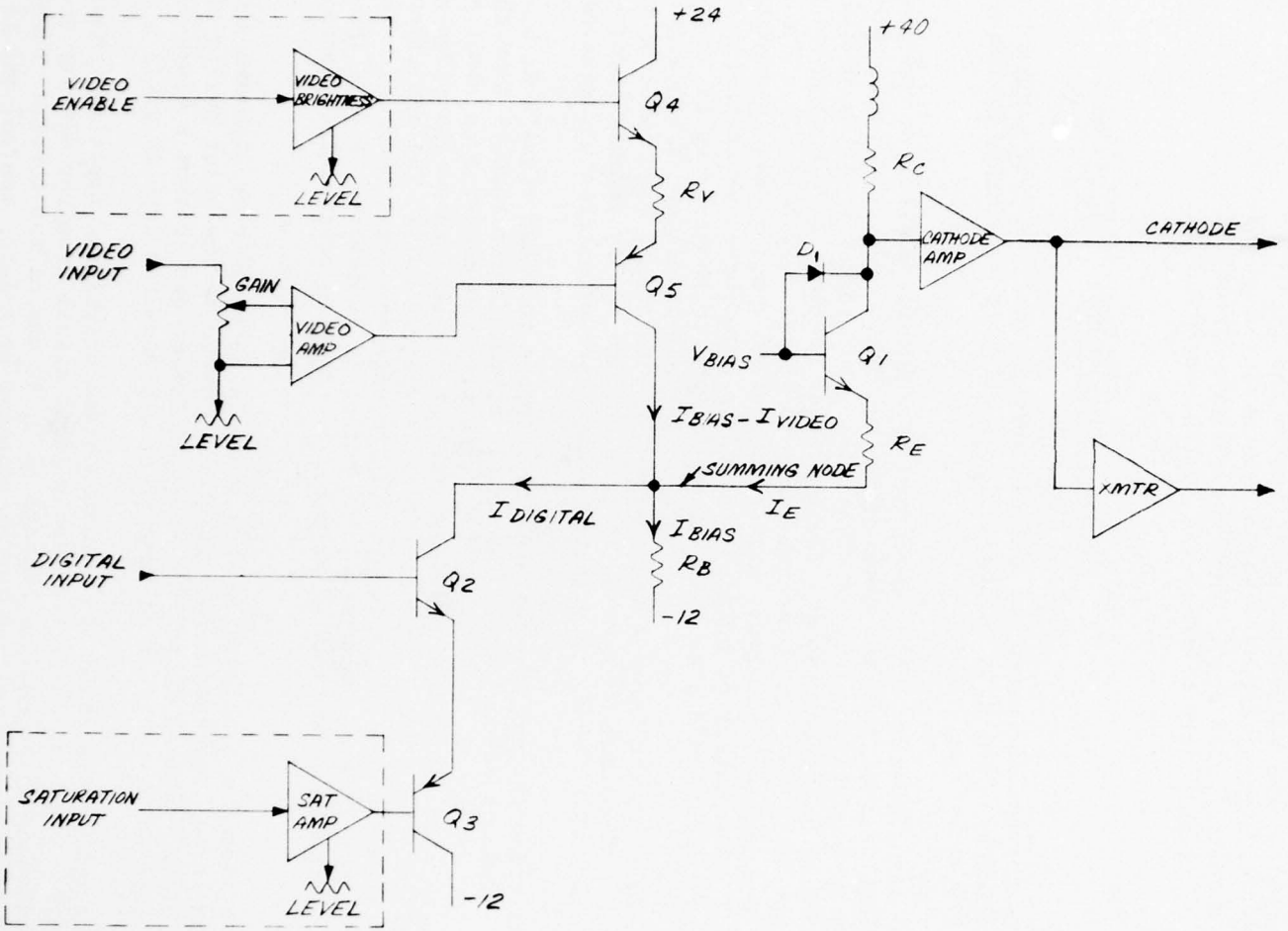


Figure 6.1 Video Amplifier

When the video is disabled this current is at a maximum of about 75 ma. This current is sunk through the bias resistor R_B, and thus the emitter current of the cathode output, Q_1, is determined wholly by the digital current as per Equation 3. When the video is enabled by the emitter voltage of Q_4, the collector current of Q_5 decreases with the increasing video signal from about 75 to about 25 ma at full video signal. There is no digital current during this event (Q_2 is cut off), so the emitter current of Q_1 and hence the cathode output voltage is determined by the bias current and the collector current of Q_5. Since the bias removes about 75 ma from the summing node, the emitter current of Q_1 varies from 0 to about 50 ma at maximum video signal, sufficient to drive the cathode to full intensity.

The level control on the video brightness amplifier controls the emitter voltage of Q_4 and hence the collector current of Q_5. This control is used to vary the video intensity independently of the digital intensity.

The output voltage developed at the collector of the common-base amplifier is buffered by the cathode amplifier. Slight peaking of the output voltage is done by a small, $\approx$ 2 μh, inductance in the collector load.

This amplifier consists of a complementary pair of emitter-follower transistors biased slightly into Class A operation to avoid crossover distortion. The cathode amplifier has a voltage gain of 1 and serves to convert the relatively high output impedance of the amplifier Q_1 into low impedance suitable for driving the cathode capacitance of about 15 pf at the video and data rates. The current required to charge and discharge this capacitance in 20 nsec is about 25 ma, which is supplied and sunk by the cathode amplifier. This amplifier also supplies a drive of up to 10 ma to the transmitter.

There are three transmitters in the video system. These convert the R, G, and B information at the cathode into signals for retransmission to other displays. One transmitter is shown in Figure 1. This converts the cathode voltage swing of +5 to +40 volts into a voltage of 1 to 0 volts, respectively, at an impedance capable of driving 75 ohm coaxial cable. The transmitter consists of a divider, an inverting amplifier, and an emitter follower. The maximum output voltage can be adjusted from the nominal 1 volt level to about a maximum of +6 volts. The output is a black negative signal similar to RS-170 standards. The frequency response of the transmitter is sufficient to make the transmitted signal an exact reproduction of the cathode voltage in the originating display.

7.0 SOFTWARE/HARDWARE OPERATION PROCEDURES

The operational procedures of the color display microcode are broken up into four major categories: keyboard operations, which is the entering and editing of alphanumeric data; graphics, which is the creation and editing of graphic items; tape operations, which permits the user to save graphic tables and programs on cassette tape; and color.

Before the user can use any of these functions he must load and initialize the system. This is done by:

1. Turning on the display unit. (The switch is on the back panel of the unit.)

2. Turning on the cassette tape drive. (The switch is on the front panel of the unit.)

3. Inserting a cassette tape that has the operational program on it.

4. Pressing INIT.

For INIT, all four pages of character memory are set to unprotected blanks with a color code of 0 (black). All tabs are cleared. Page 0 is displayed. The cursor is set to the home position, i.e., the upper left-hand corner of the screen. The mode keys are set to UNPROTECTED and REPLACE. GRAPHICS ACTIVE is turned off.

7.1 KEYBOARD OPERATIONS

This section includes all operations which are used to enter and edit alphanumeric data on any one of four pages, a page being 25 rows by 80 columns. A description of two conditions, wrap-around and hidden memory, which the user should be aware of before doing any detailed editing, precedes the explanation.

7.1.1 Wrap-Around

A wrap-around is the process of repositioning alphanumeric data used in certain editing functions in character memory (and therefore, on the screen). It is intended to duplicate, or at least to approximate, the arrangement that follows the rules of spacing for typed text with left justification and to minimize space filling at the right margin. It does not right justify text or hyphenate words not previously hyphenated.

The editing functions that use the wrap-around are, in the REPLACE mode, WORD DELETE, RUB OUT, CHARACTER DELETE, COPY, and MOVE; and in the INSERT mode, all of these plus DELETE BETWEEN MARKS and the character keys, the space bar, and MARK, if the right-most column of the row where the character is being inserted is not blank.

A wrap-around may affect either one or two segments of text. One of these, the marked text, is the contiguous set of characters between two marks.

The marks need not be on the displayed page. The other segment, the wrapped text, is the contiguous set of characters that starts at a position that depends on the editing function in use and ends at whichever of the following is encountered first by a forward scan of the text: (1) the last nonblank character preceding a protected character, (2) the last nonblank character preceding a blank in the left-most column, (3) the last nonblank character on the page. Wrapped text may have embedded marked text; if it does, the boundaries of both are unaffected.

Marked text can be wrapped into any unprotected area of the screen, starting at the cursor position. Wrapped text can be wrapped into any unprotected area of the screen that starts at the cursor position and ends at a wrap boundary that depends on which of the above three conditions terminated the wrapped text. If (1), the wrap boundary is the position preceding the protected character; if (2), the end of the row preceding the blank in the left-most column or the end of the last consecutive all blank row immediately following that position; if (3), the end of the screen. Text that would wrap past the wrap boundary causes an alarm.

These rules are intended to preserve paragraphing in a wrap-around and to exclude tabular data not using the left-most column from a wrap-around. Nevertheless, marked text may (in REPLACE mode) be wrapped into the next paragraph or over tabular data.

The smallest unit of text moved in a wrap-around is one word. A word boundary can be a blank, hyphen, slash, blink, reverse video character, or either end of a row. A single blank character is assumed to exist between the word at the end of one row and the word at the beginning of the next, with certain exceptions. If the last non-blank character in a row is a blink, reverse video, hyphen, or slash, no additional blank is inserted between the words. If the last nonblank character in a row is a period, question mark, or exclamation mark, two blanks are inserted. In all cases, however, no blanks are required between words wrapped into different rows. Blanks at the right end of a row of marked or wrapped text are suppressed if they exceed the number required by the above rules.

A series of contiguous blanks in wrapped or marked text may be reduced in number if the wrap-around moves them to the end of a row. Hence, space intended for future entries should be filled temporarily with dummy characters before a wrap-around.

7.1.2 Hidden Memory

Each page of memory consists of the 24 rows of characters displayed on the screen plus a 25th row at the bottom, which is not displayed. This hidden row can be written only by the NEW LINE and CLEAR functions and can be read only by the LINE DELETE function and by a wrap-around which moves data up (as in WORD DELETE, CHAR DELETE, RUB OUT, and DELETE in the INSERT mode). The NEW LINE key can shift data from the 24th row into the hidden row. The LINE DELETE key can shift data from the hidden row into the 24th row. The CLEAR key stores blanks into all unprotected locations from the cursor position forward to the end of the hidden row. The DELETE, MOVE, and COPY keys may use marked text from the hidden row.

7.1.3 Data Entry Keys

7.1.3.1 Character Keys and Space Bar in the REPLACE Mode - The keyed-in character (or a blank for the space bar) with the color selected by the color keys is stored at the cursor position, overwriting the character previously at that position. The cursor is advanced to the next unprotected position.

ALARMS - None.

7.1.3.2 Character Keys and Space Bar in the INSERT Mode - If there is a blank in the right-most column of the row at the cursor position, the characters under and to the right of the cursor are shifted right one column. Then the keyed-in character or blank with the color selected by the color keys is stored at the cursor position. If the right-most column of the row at the cursor position is not blank, the insertion causes a wrap-around of the text starting at the first character of the word at the cursor position and including the inserted character. The cursor is repositioned to follow the inserted character. This may be either one column to the right of the original position or in the next row.

ALARMS - (1) A character in the row at the cursor position and at the right of the cursor is protected. (2) Text would be wrapped into a protected field. (3) Text would be wrapped past the wrap boundary.

7.1.4 Cursor Controls

The CURSOR HOME key moves the cursor to the upper left hand corner of the screen or to the first unprotected position found by scanning from left to right, top to bottom. The four keys labeled with arrows move the cursor in the indicated directions. The move is to the adjacent position in the direction designated by the key, if the key is held for less than 0.5 seconds. It moves continuously at 20 positions per second if the key is held down. If a move encounters a protected position, the cursor skips over it in the same direction until it reaches an unprotected position. Vertical moves wrap around from the bottom to the top of the screen, or top to bottom, with no horizontal shift. Horizontal moves wrap around from the left side of the screen to the right side with a shift one row up, and from the right side to the left side with a shift one row down. Continuous diagonal motion results from holding one vertical and one horizontal key.

7.1.4.1 MARK in REPLACE Mode - A special character is stored in character memory at the cursor position, overwriting a character previously at that position, and the cursor is advanced to the next unprotected position.

ALARMS - None.

7.1.4.2 MARK in INSERT Mode - The same special character is written at the cursor position and following characters are shifted as described under character keys, INSERT mode. Marks are used to define segments of text for the MOVE, COPY, and DELETE functions. Marks are always unprotected, whether or not the PROTECT mode is set.

ALARMS - Same as character keys in the INSERT Mode.

7.1.4.3 ERASE MARK - If the cursor is on a mark, that mark is erased and replaced by a blank. If the cursor is not on a mark, a single ERASE MARK keystroke does nothing. If it is followed by a second ERASE MARK keystroke, all marks in the memory are erased regardless of the cursor position. An ERASE MARK keystroke is considered to be the second only if no other character or editing keys were pressed between it and the first ERASE MARK.

ALARMS - None.

Rules for Marks

1. Only one page at a time can have marks.

2. A mark entered on one page erases any marks that may have existed previously on another page.

3. Only two marks may be present on a page.

4. An attempt to enter a mark on a page already having two marks causes an alarm.

5. A mark may be entered in any unprotected position on the screen, or moved into the 25th or hidden row by a NEW LINE function.

6. Two marks not enclosing protected data are required on a page for the DELETE, MOVE, and COPY functions.

7. Both marks are erased following normal execution of a DELETE, MOVE, or COPY function, but not if there is an alarm.

8. The DELETE, MOVE, and COPY functions may use data between marks on any page, whether or not that page is the one displayed.

7.1.4.4 SET TAB - A tab is set at the column at the cursor position.

ALARMS - None.

7.1.4.5 CLEAR TAB - The tab is cleared at the column at the cursor position.

ALARMS - None.

TAB: The cursor advances from left to right until it reaches a column at which the tab is set. If that position is protected, the cursor advances to the next unprotected position to the right. If no tabs are set, the TAB key acts as a carriage return.

ALARMS - None.

7.1.5 Editing Functions

7.1.5.1 LINE DELETE - All data in the rows from one row below the cursor position to the lowest row not containing protected data are shifted up one row,

overwriting the row at the cursor position. Blanks are stored in the lowest row from which data was shifted. If there is no protected data in the rows at or below the cursor position, the shifting starts from the hidden row and blanks are stored in the hidden row. There is no wrap-around, but a straight vertical shift, permitting use with tabular data.

ALARMS - Protected data in the row at the cursor position.

7.1.5.2 NEW LINE - All data in the row at the cursor position and all rows below it are shifted down one row. The data in the bottom row of the screen are shifted into the hidden row. Blanks are stored in the row at the cursor position. There is no wrap-around, but a straight vertical shift, permitting use with tabular data.

ALARMS - (1) Nonblank characters in the hidden row, which would be overwritten. (2) Protected characters in any row at or below the cursor position.

7.1.5.3 CHARACTER DELETE - The character at the cursor position is removed, and text to the right of it is word-wrapped to the cursor position. If the last nonblank character in a row, or any blank to the right of it, is deleted, the wrapped text starts at the left-most column of the next row and is wrapped to the position one column to the right of the cursor.

ALARMS - None.

7.1.5.4 RUB OUT - The character one column to the left of the cursor position is removed. The cursor is set to the position of the removed character. Text to the right of the removed character is word-wrapped to the new cursor position. If the last nonblank character in a row, or any blank to the right of it, is deleted, the wrapped text starts at the left-most column of the next row and is wrapped to the position one column to the right of the cursor.

ALARMS - (1) The character at the left of the cursor position is protected. (2) The cursor is in the left-most column.

7.1.5.5 WORD DELETE - If the cursor is on a blank, blink, reverse video, or mark, nothing happens. Otherwise, the word at the cursor position is deleted and the text starting at the next nonblank character is word-wrapped into the position of the deleted word. The word boundaries for deletion are slightly different than for wrap-around. For deletion, a blank, blink, reverse video, mark, protected character, or either end of a row constitutes a word boundary. A hyphen or slash does not. If the wrap-around following word deletion would bring two blinks or two reverse videos together, they too are deleted before the wrap-around.

ALARMS - None.

7.1.5.6 COPY in REPLACE Mode - Only the marked text is moved. It is wrapped into the area of the screen, starting at the cursor position. It overlays the data originally in the area required for wrapping the marked text, whether or not that area contains a blank in the left-most column of any row. The

marks are erased, but not the text between them. The cursor remains in the original position. If the text being copied occupies more than one line in the new location, the line divisions will be made according to the same rules that the wrap-around uses for line divisions, i.e., at a blank, blink, reverse video, hyphen, or slash. If such a division leaves unoccupied columns at the right end of a line other than the last, they are blank-filled.

ALARMS - (1) Two marks are not present. (2) The marks enclose protected data. (3) Text would be wrapped into a protected field. (4) Text would be wrapped past the end of the screen.

7.1.5.7 MOVE in REPLACE Mode - Same as COPY in the REPLACE Mode, except that the text between marks is erased (provided both marks remain after the wrap-around).

ALARMS - Same as COPY in the REPLACE Mode.

7.1.5.8 COPY in INSERT Mode - Two segments of text are affected, the marked text and wrapped text, as defined in paragraph 7.1.1 on the wrap-around. A combined segment is formed from these two, with the marked text first and wrapped into the area of the screen starting at the cursor position. Normally, the wrapped text will extend beyond the area it originally occupied. It must not extend beyond the wrap boundary, as defined in paragraph 7.1.1 on the wrap-around. After wrap-around, the marks are erased, but not the text between them. The cursor remains in the original position.

ALARMS - (1) Two marks are not present. (2) The marks enclose a protected byte. (3) Text would be wrapped into a protected field. (4) Text would be wrapped past the end of the screen. (5) Text would be wrapped past the wrap boundary.

7.1.5.9 MOVE in INSERT Mode - Same as COPY in INSERT Mode, except that if two marks remain anywhere on the screen after the wrap-around, all text between them is erased.

ALARMS - Same as COPY in INSERT Mode.

7.1.5.10 DELETE in REPLACE Mode - The two marks and the text between them are replaced by blanks with a color code of 0 (black).

ALARMS - (1) Two marks are not present. (2) The marks enclose a protected character.

7.1.5.11 DELETE in INSERT Mode - The text following the second mark is wrapped into the area starting at the first character of the marked text. The first mark is erased.

ALARMS - (1) Two marks are not present. (2) The marks enclose a protected character.

7.1.6 Character Modes

7.1.6.1 REVERSE VIDEO - The first time this key is depressed a reverse video character is entered into character memory, and all characters after this are black characters on this respective colored background. The second time this key is depressed another reverse video character is put into character memory, thus, terminating the reverse video of the text. All text which is reverse video can be edited without affecting the reverse video Naturally, the reverse video character pairs must be maintained to keep the intended effect.

7.1.6.2 CHARACTER BLINK - The same applied to character blinking as reverse video, except a character blink code is put in character memory and the text between character blink codes is blinked once per second.

7.1.6.3 CLEAR - All unprotected characters from the cursor position to the end of the hidden row are replaced with blanks having a color code of 0 (or black).

ALARMS - None.

7.1.6.4 NEXT PAGE - Displays the text contained in the next page of memory, i.e., the next 25 lines of character memory, the 25th being hidden. The cursor is placed in the first nonprotected character position.

ALARMS - If the current page is the last page, the alarm sounds and the last page remains displayed.

7.1.6.5 PREVIOUS PAGE - Displays the text contained in the previous page of memory. The cursor is placed in the first nonprotected character position.

ALARMS - If the current page is the first page the alarm sounds and the first page remains displayed.

7.1.6.6 PROTECT - Any text except MARK entered in this mode can no longer be accessed or edited. It is a permanent part of character memory and can't be changed. A mark is never protected.

7.1.6.7 KEYBOARD ALARM - This lights whenever an illegal procedure has been executed by the user during a keyboard (nongraphic) function. Before any more keyboard entries can be made, the alarm condition must be turned off by depressing the ALARM key.

7.1.6.8 INSERT/REPLACE - Selects the mode of operation for character keys, MARK, COPY, MOVE and DELETE.

7.2 GRAPHICS

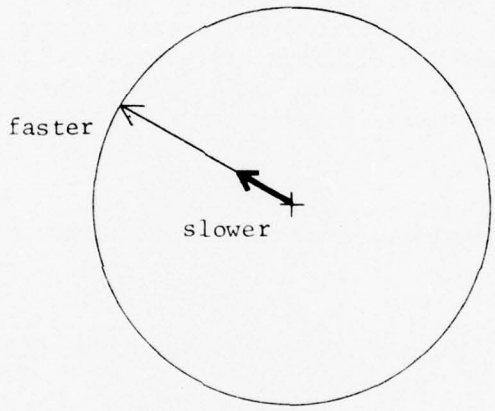
This section describes the procedures used to create and edit graphic items. To put the display into a graphic mode the user must press Graphics Active.

7.2.1 GRAPHICS ACTIVE

This takes the program from alphanumeric mode to a graphics mode. The alphanumeric cursor is buried in the hidden line and the graphics cursor or crosshair is put at the home position, the center of the screen. Graphic items on the screen and in the graphics tables are not altered. Once the crosshair is at home position it can be controlled by the joystick.

7.2.2 GRAPHIC CURSOR CONTROL

The graphic cursor is controlled by the joystick. The joystick is a device that looks much like a toggle switch except it is free to move to any position on a 360° circle. When the joystick is moved to a given position, the cursor moves in that direction at a rate proportional to its distance from the center. An illustration of this is:



7.2.3 GRAPHICS MARK

Once the cursor is positioned at the desired coordinate, the user relates to the program that the cursor is positioned by pressing GRAPHICS MARK. This is a fundamental part of all graphics use because this is how coordinates for various functions are interactively entered.

7.2.4 ENTER 2ND INDICATOR

This is lighted whenever a function requires two or more coordinates to be entered to complete a function. When the function is completed, it is extinguished.

7.2.5 ERROR INDICATOR

This is lighted whenever an input to a given graphics function is in error.

7.2.6 BELL

The bell sounding in conjunction with the error light indicates the graphics table can hold no more data.

7.2.7 CLEAR GRAPHICS

This does a full screen erase of graphics memory and reinitializes the graphics tables. Note: All graphics are lost.

7.2.8 RESTORE GRAPHICS

This does a full screen erase and then restores all current graphic items in the order they were created. The graphics tables are unaffected. Note: This is extremely useful when editing graphics.

7.2.9 GRAPHIC OPERATIONAL PROCEDURES

There are five basic functions which can be used to work with a graphic item. The functions are Generate, which creates new graphic items, and Blink, Restore, Erase, and Saturate, which are used to edit existing graphic items. A graphic item can be any of four conic types: Vector, Vector String, Arc, and Circle. An illustrative overview of the command structure is as follows:

FUNCTION

(Generate, Restore, Erase, Blink, Saturate)

CONIC

(Vector, Vector String, Arc, Circle)

INPUT STEP

(Marks)

The command structure works top down until the user starts entering marks, i.e., the user can change his choice at the upper two steps but once he enters an input step he must follow through. A description of all conic function input steps are as follows:

7.2.9.1 GENERATE - This function is used to create all new graphic items. If this is the desired function, the user must then select the conic he wishes to create.

7.2.9.1.1 VECTOR - This draws a line from (X1, Y1) to (X2, Y2)

MARK 1 - Defines the location of (X1, Y1). The color must be specified before this mark.

MARK 2 - Defines the location of (X2, Y2). The line is drawn at this time.

ENTER 2ND - Is turned on after MARK 1 and extinguished after MARK 2.

ERROR - Is lit and the bell sounds when there is no room in the graphics tables for the vector. The operator should note that even though the vector is displayed, it is not a part of the picture. To erase the vector, press Restore Graphics.

7.2.9.1.2 VECTOR STRING - This draws a vector string from (X1, Y1) to (X2, Y2) to ... to (Xn, Yn). N = 2,3,...1420(10).

MARK 1 - Defines the location of (X1, Y1). The color must be specified at any time before this mark.

MARK 2 - Defines the location of (X2, Y2).

MARK (n-1) - Defines the location of (X(n-1), Y(n-1)).

MARK n - Doesn't really exist because the program has no way of distinguishing it as the last mark. Thus, a unique key, called the End Vector String, must be used. It works like a mark in that it defines the cursor position, but it also serves to tell the display to terminate the vector string. When End Vector String is pressed, the program compares the first point with this last point and if they're less than 6 rasters apart the last point is set equal to the first point. This second feature will be apparent when saturation is discussed. (See paragraph 7.2.9.5.)

ENTER 2ND - Is lit after Mark 1 and is extinguished after End Vector String.

ERROR - Is lit and the bell sounds when there is no room in the graphics tables for the vector string. Like a vector, the vector string is lost even though it is displayed.

7.2.9.1.3 CIRCLE - Draws a circle with a radius (X2, Y2) about a center (X1, Y1)

MARK 1 - Defines the location of the center (X1, Y1).

MARK 2 - Defines the radius of the circle. The color must be specified before this mark.

ENTER 2nd - Is lit after Mark 1 and is extinguished after Mark 2.

ERROR - 1) If the radius is greater than 255 rasters.
2) If the radius is less than 5 rasters.

Note: If the radius is either too small or too large, reposition the cursor and press MARK. This takes the place of Mark 2.

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COLOR TERMINAL DEVELOPMENT STUDY.(U)
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UNCLASSIFIED RADC-TR-77-271 NL

2 OF 2
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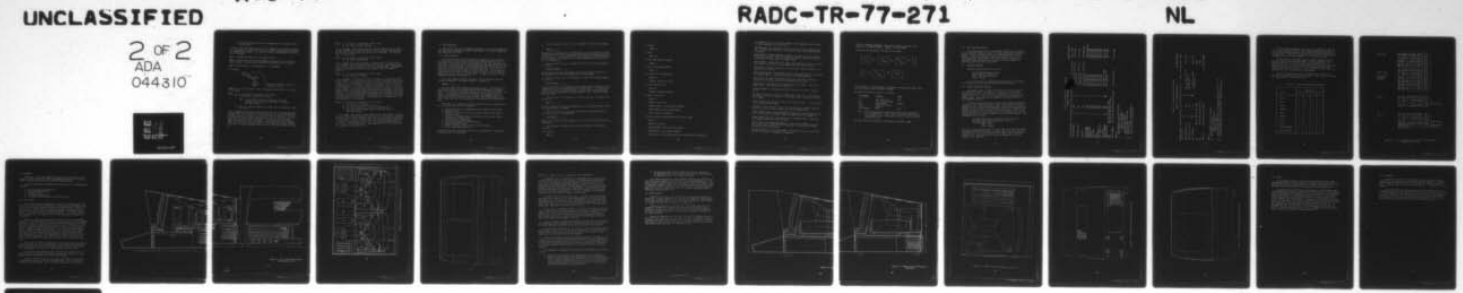
044310



END
DATE
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10-77
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3) With bell indicates there is not enough room in the graphics table for the circle.

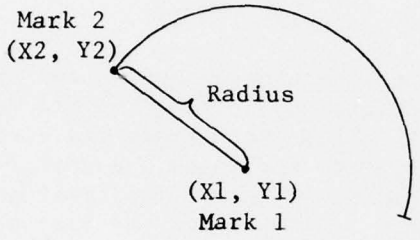
7.2.9.1.4 ARC - This draws an arc in 7 1/2° segments in a clockwise direction at 1 seg/sec about a center (X1, Y1) from a segment containing (X2, Y2) until the third mark is entered. If it draws a circle, it automatically stops without a third mark.

MARK 1 - Defines the location of the center (X1, Y1).

MARK 2 - Defines the radius and the segment containing (X2, Y2) in which to start drawing. The color must be specified at any time before this mark.

MARK 3 - Defines when to stop drawing the 7 1/2° segments.

For example:



Mark 3 at this point stops the drawing of the arc.

ENTER 2nd - Is lit after Mark 1 and is extinguished after Mark 3 or if a 360° arc is drawn.

ERROR - 1) If the radius is greater than 255 rasters.
2) If the radius is less than 5 rasters.

Note: If the radius is either too small or too large, reposition the cursor and press MARK. This takes the place of Mark 2.

3) With bell indicates there isn't enough room in the graphics table for the arc.

7.2.9.2 BLINK - This function serves two purposes: one is drawing the user's attention to a particular event on the screen, and the second is identifying a graphic item to be edited, i.e., erased, restored, or saturated. If this is the desired function, the user must select the conic he wishes to blink. He then places the cursor within 5 rasters of the desired conic and presses MARK. The entire conic will then begin to blink (except for vector strings, where only the first vector will blink). If the wrong item blinks, restore it and try to blink the desired conic with the cursor more optimally positioned.

ERROR - 1) The cursor is outside the 5 raster limit.
2) The item is already blinking.

7.2.9.3 RESTORE - This function restores a given blinking item. If this is the desired function the user must select the conic that is blinking, position the cursor with 5 rasters of the item, and press MARK. The blinking conic is then restored.

ERROR - 1) The cursor is beyond the 5 raster limit.
2) The item is not blinking.

7.2.9.4 ERASE - This function erases a blinking item. If this is the desired function, the user must then select the conic that is blinking, position the cursor within 5 rasters of the item, and press MARK. The blinking item is then erased and its entry in the graphics table is flagged for deletion.

ERROR - 1) The cursor is beyong the 5 raster limit.
2) The item isn't blinking.

7.2.9.5 SATURATE - This function fills in or shades in circles and closed vector strings. A closed vector string is a vector string whose first point is equal to its last endpoint and has no point where it crosses itself, i.e., a mathematically closed polygon. Shading can be done in any color at full or half intensity. If shading is desired, the user must select a circle or vector string as a conic, position the cursor within 5 rasters of the item, and press MARK. The blinking item is then restored and shaded. Color can be chosen at any time before the MARK, and intensity is controlled by the highlight key. For full intensity the highlight key must be pressed after saturation is selected and before MARK. If the shade is not as desired, the user can blink the item and saturate it a different color. Intensity is half if the highlight key is not pressed.

ERROR - 1) The cursor is beyond the 5 raster limit.
2) The item isn't blinking.
3) The conic chosen was an arc or vector.
4) The vector string wasn't closed or crossed itself.
5) With bell indicates there wasn't enough free space for saturation tables.

7.2.9.6 COLOR - This section briefly describes the color cluster. For the most part, these buttons instantly change the color of whatever is being done on the display. The only time this isn't true is after the first mark when creating vectors or vector strings, after the second mark when creating arcs or circles, or whenever the user is not at a step in the tape operations. Once a color has been selected, all user inputs will be in that color until it's changed to a different color.

7.3 TAPE OPERATIONS

This section includes all commands necessary for the user to communicate the desired use of the cassette tape to the display. To use this feature the user must press INIT TAPE.

7.3.1 Tape Procedures

To use the cassette, the user must put the alpha cursor at a place on any page where the tape routines can have five consecutive lines to use as work space. If the user has the cursor anywhere on the last five lines, the bottom five lines will be used. It should be noted that the contents in this work space will be destroyed. Before initiating tape action be sure the cassette unit is powered on and that the desired tape is in. If it is to be read only, put on the file protect. Now press TAPE INIT. The routines will then initialize the cassette hardware, rewind the tape, and try to read the TOC$$$ block (first block on a blocked tape). If there is no TOC, an error message to that affect is written.

All future requests from the controller will be answered by the user through the keyboard. The general format of a request is:

REQUEST = _____

The user types in his response and carriage return. If he makes a mistake before pressing CR, he presses Rub Out and the request will be made again. If at any time the routines encounter an error while processing a request, an error message describing the problem will be typed out on the screen. An alphabetical list of error messages and suggested courses of action can be found at the end of this section. The following step is the basic control step that is the beginning of any tape action or tape related task.

When MODE = ___ is written in the work space, the user can respond with any of the following upper case responses:

A - Absolute write for load programs that are read by the ROM loader.
B - Rewinds the tape.
E - Rewinds the tape and exits from the tape routines to the general executive state.
G - Displays the contents that are currently in the graphics tables; initiates all blinking items.
I - Initializes the cassette unit.
P - Positions the tape at the desired block.
R - Reads the desired block.
T - Prints the table of contents by ID and date written.
W - Writes a desired block of data.

If the user types any other character it will be considered as invalid and the question will be asked again.

The second step to an A, P, R, or W response is to ask for the program ID.

PROGID = _____

The program ID, consisting of six alphanumerics, is left justified and blank filled. If this is a P or R operation, this identifies the desired block as is in the TOC. If no ID can be found, an error message is given and it asks for the ID again. In the case of A or W this identifies the ID the block will be referenced by.

The third step of an A or W respose is to ask for the starting address of the data.

STARTING ADDRESS = _____

The user must enter the octal address, which cannot exceed six digits. If the response was in error, the question will be asked again.

The fourth step of an A or W response is to ask for the ending address of the data.

ENDING ADDRESS = _____

The user must enter the octal address which cannot exceed six digits. If the response was in error, the question will be asked again. If the ending address was less than the starting address, an error occurs and the user must re-enter the *starting address and ending address.* Note: Never use an address over 67500.

The fifth step of a W response is to ask for the date if it hasn't been entered yet.

DATE = _____

The date consists of up to six alphanumerics, left justified and blank filled. The suggested format is MMDDYY.

The fifth step of an A response is asking the load address where the data block is to be loaded when read.

LOAD ADDRESS = _____

The user must enter the octal address; if it's in error the question will be asked again.

Some examples of the steps a user would go through to do a desired task are:

To initialize:

MODE = I

To rewind:

MODE = B

To exit:

MODE = E

To print the table of contents:

MODE = T

To draw from graphics tables:

MODE = G

To position at a desired block:

MODE = P

PROGID = (desired block ID)

To read a desired block:

MODE = R

PROGID = (desired block ID)

To write a data block:

MODE = W

PROGID = (block ID)

STARTING ADDR = (octal starting address)

ENDING ADDR = (octal ending address)

DATE = (date block written)

To write an absolute program which can be read by ROM:

MODE = A

PROGID = (block ID)

STARTING ADDR = (octal starting address)

ENDING ADDR = (octal ending address)

LOAD ADDR = (octal addr where ROM will load the absolute program)

An alphabetical list of the error messages, their meanings, and the course of action suggested for each follows.

BAD CHECK SUM - The check sum on the tape did not match the computed check sum. Processing of this data is at the user's risk. (The block should be read again.)

BLOCK LENGTH IS SHORTER THAN DATA IN BLOCK - The actual data on the tape is shorter than expected. This can probably be ignored, but if the user has problems with the data, this is a likely cause.

CAN NOT WRITE - Either there is no tape or the file protect is set. Fix the tape problem, initialize, read the TOC$$$ block, position, and write.

DUPLICATE ID - There is already an ID by this name. Choose a unique ID for the block to be written.

ENDING ADDR MUST BE GE TO THE STARTING ADDR - The ending address is less than the starting addres . Reenter the starting and ending addresses.

EOT - ABORT - The tape has gone beyond the end of tape mark. Rewind; if reading or positioning, there was not enough room on the tape.

INVALID MODE - The response to the mode request was invalid. Reenter the mode; be sure you're using upper case keys.

INVALID PROGRAM ID - The program ID didn't match any in the TOC. Reenter the ID.

NO EOF$$$ IN THE TOC - There is no EOF$$$ entry in the TOC. You'll have to put EOF$$$ in the TOC by hand with a maintenance panel. There should always be an EOF$$$.

NO TOC - Either the tape has no TOC or there was a bad read. If you expected a TOC, REWIND and READ TOC$$$.

NOT READY - Either the unit is not on or the tape is not inserted correctly. Solve the problem, initiate, rewind, and read the TOC$$$ block.

PARITY ERROR IN BLOCK - SUGGEST REREADING - There was a parity error with the IRG. Use the data at the user's risk; rereading the block is suggested.

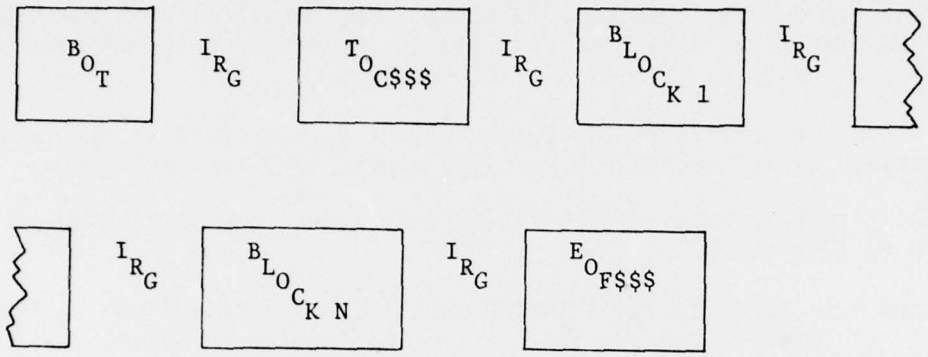
PARITY ERROR IN THE DATA - The tape unit will continue reading. There was an incomplete read on a word in the data.

PARITY ERROR IN THE HEADER-READ ABORTED - There was an incomplete read on a word in the header, and the read was terminated. Since no data was read, the user must reread the block.

REQUESTED PROGRAM ID COULD NOT BE FOUND - The requested block was in the TOC but not on the tape. A rereading is suggested.

THERE IS A NONOCTAL CHARACTER - There was a nonoctal character in the response to an address request. Reenter the octal number.

The basic block structure of the tape is as follows:



The structure of an absolute tape is the same as a blocked tape except there is only one block, with no TOC$$$ or EOF$$$.

The basic structure of a block is as follows:

Word Number	Contents	Type
0	BOR - 0375 code	BOR
1-6	Six character header	
7,8	Load address	Header
9,10	Length of the data	
11,12	Check sum	
13-(12+length)	DATA	Data

NOTE: When a blocked tape is being written, there are several BORs at the beginning of a block. This is to insure that the block can be properly read. The purpose of this is to put the read operation in sync.

Free table space or the graphics tables range from 32000 - 67500.

8.0 HOST COMPUTER INTERFACE

In the development of the color display terminal a host computer was not required. Because of this and because the hardware required for possible interfaces already existed, no further development was done. However, a study was completed to determine the effect of color on existing systems. Specifically, the U-1652 system was examined for compatibility and requirements for expansion of data exchanges to handle the additional color information.

8.1 INTERFACE HARDWARE

Currently existing interface cards are:

MIL-STD-188-100 balanced serial
MIL-STD-188C low level serial
NTDS - fast 8-bit parallel
RS-232 - serial

As has been stated, no interface has been included in the design of the U-1655, but provisions for interfaces have been made.

8.2 MESSAGE FORMAT AND PROTOCOL

The message format for the U-1655 must have as little impact on existing U-1652 systems as possible. To achieve this end, message format and protocol for the U-1655 will be identical to the U-1652, except in two areas: character color identification and graphic color identification. Tables 8.1 and 8.2 summarize the data transfers of the recommended protocol.

The basic message consists of at least four synchronous idle bytes followed by a Data Link Escape (DLE), Start of Text (STX), and three identifier bytes: Remote Identifier (RID), which identifies the specific terminal on that processor; Site Identifier (SID), which identifies the specific terminal on that processor; and Device Identifier (DID), which identifies the device on the terminal that is being addressed. The RID and SID identifiers are switch selectable in each display terminal. Code assignments are as follows:

RID CODES 040 thru 047 (Terminal processor 0 thru 7)
SID CODES 0120 thru 0157 (Terminal 0 thru 31)
DID CODES 0160 - Display
0161 - VFK
0162 - Graphics

The text is bracketed by the Start of Text (STX), Data Link Escape (DLE), and End of Text (ETX) characters. All bytes are 8 bits with no parity. The eighth bit is used for protected field. NAK is sent to indicate a message error. ACK response is for any text message which does not require a text response.

Table 8.1 Display Int[illegible] Formats

	COMPUTER TO DISPLAY [illegible]ES		DISPLAY RESPONSE
POSITION CURSOR	SYN SYN SYN SYN DLE STX RID SID DID[2] STX	ESC q X Y DLE SI DLE ETX	ACK or NAK
LOAD DISP MEM 3	DLE	ESC Y XI YI XF YF[6] DLE SI DATA DLE ETX	ACK or NAK
LOAD INIT MEM 4	DLE	ESC u XI YI XF YF[6] DLE SI DATA DLE ETX	ACK or NAK
REQ MEM	DLE	ESC s XI YI XF YF[6] DLE SI DATA DLE ETX	SEND MEM DATA
SENSE CURSOR	DLE	ESC C DLE ETX	SEND CURSOR POS.
CLEAR SCREEN	DLE	ESC P DLE ETX	ACK or NAK
MASTER CLEAR	DLE	ESC B DLE ETX	ACK or NAK
TAB SET	DLE	ESC H DLE ETX	ACK or NAK
TAB CLEAR	DLE	ESC J DLE ETX	ACK or NAK
TAB	DLE	ESC I DLE ETX	ACK or NAK
ALARM	DLE	ESC T DLE ETX	ACK or NAK
KBD LOCKOUT	DLE	ESC L DLE ETX	ACK or NAK
L.P. INT. LIGHT	DLE	ESC F DLE ETX	ACK or NAK
VFK LIGHTS	DLE	LVFK[5] RVFK[5] DLE ETX	ACK or NAK
GRAPHIC COMMAND	DLE	ESC G DATA DLE ETX	ACK or NAK
CLEAR GRAPHICS	DLE	ESC P DLE ETX	ACK or NAK
ACK	SYN SYN SYN SYN ACK (26Ø)		
NAK	SYN SYN SYN SYN NAK 0 (NULL)		
COLOR COMMAND	SYN SYN SYN SYN DLE STX RID SID DID[2]	ESC X DATA DLE ETX	ACK or NAK

NOTES:
1. NAK response for invalid messages
2. DID = 0160 for Display
   = 0161 for VFK lights
   = 0162 for Graphics
3. Row/Column Addressing
4. Absolute Binary Addressing
5. Five Byte Code
6. XI YI = Two Byte Initial Address,
   XF YF = Two Byte Final Address

Table 8.2 Computer Interface Formats

	DISPLAY TO COMPUTER MESSAGES																COMPUTER RESPONSE
CURSOR POSITION (& L.P. INT)	SYN	SYN	SYN	SYN	DLE	STX	RID	SID	DID	STX	ESC	C	X	Y	DLE	SI	DLE ETX	ACK or NAK
SEND MEMORY DATA 3,4						STX					ESC	s	XI	YI	XF	YF[5]	DLE SI DATA DLE ETX	ACK or NAK
SEND (unsolicited) 4						STX					DATA DLE ETX							
VFK & OVERLAYS						STX					L. OVERLAY R. OVERLAY KEY DLE ETX							ACK or NAK
ACK	SYN	SYN	SYN	SYN	ACK (26Ø)													NONE
NAK	SYN	SYN	SYN	SYN	NAK Ø (NULL)													NONE
BOOT REQ	SYN	SYN	SYN	SYN	ENQ (205)													LOAD INST MEMORY

NOTES:
1. NAK RESPONSE for invalid messages
2. DID = 0160 for Display
   = 0161 for VFK & Overlay
   = 0162 for Graphics
3. Absolute Binary Addressing for Instruction Memory (upper bit = 0)
4. Row/Column Addressing for Display Memory (upper bit = 1)
5. XI YI = Two Byte Initial Address, XF YF = Two Byte Final Address

Of the transfers identified, only the color command is in addition to the U-1652 message transfers. This transfer should be sent only to a color terminal only when the character information being transferred is to change color. Character data that is received by the U-1655 is always displayed in the color last received in a color command message.

Of the transfers identified, only the graphic command is altered from the original U-1652 message formats. The only change that has been made is that the color information for each graphic type, i.e., vector string, arc, or circle, has been added to the message. This color identification is done with bits which are unassigned in the U-1652 transfers, as shown in Figure 8.1. The inclusion of the color bits will have no effect on U-1652 operation or performance.

The color information is always included in the upper bits of the first Y coordinate received for that graphic type. Table 8.3 defines the interpretation of those upper bits.

Table 8.3 Color Information Interpretation

Color	bit of Y			
	2^{12}	2^{13}	2^{14}	2^{15}
Black	X	0	0	0
Red	X	0	0	1
Green	X	0	1	0
Yellow	X	0	1	1
Blue	X	1	0	0
Magenta	X	1	0	1
Cyan	X	1	1	0
White	X	1	1	1
Full Intensity	0	X	X	X
Half Intensity	1	X	X	X

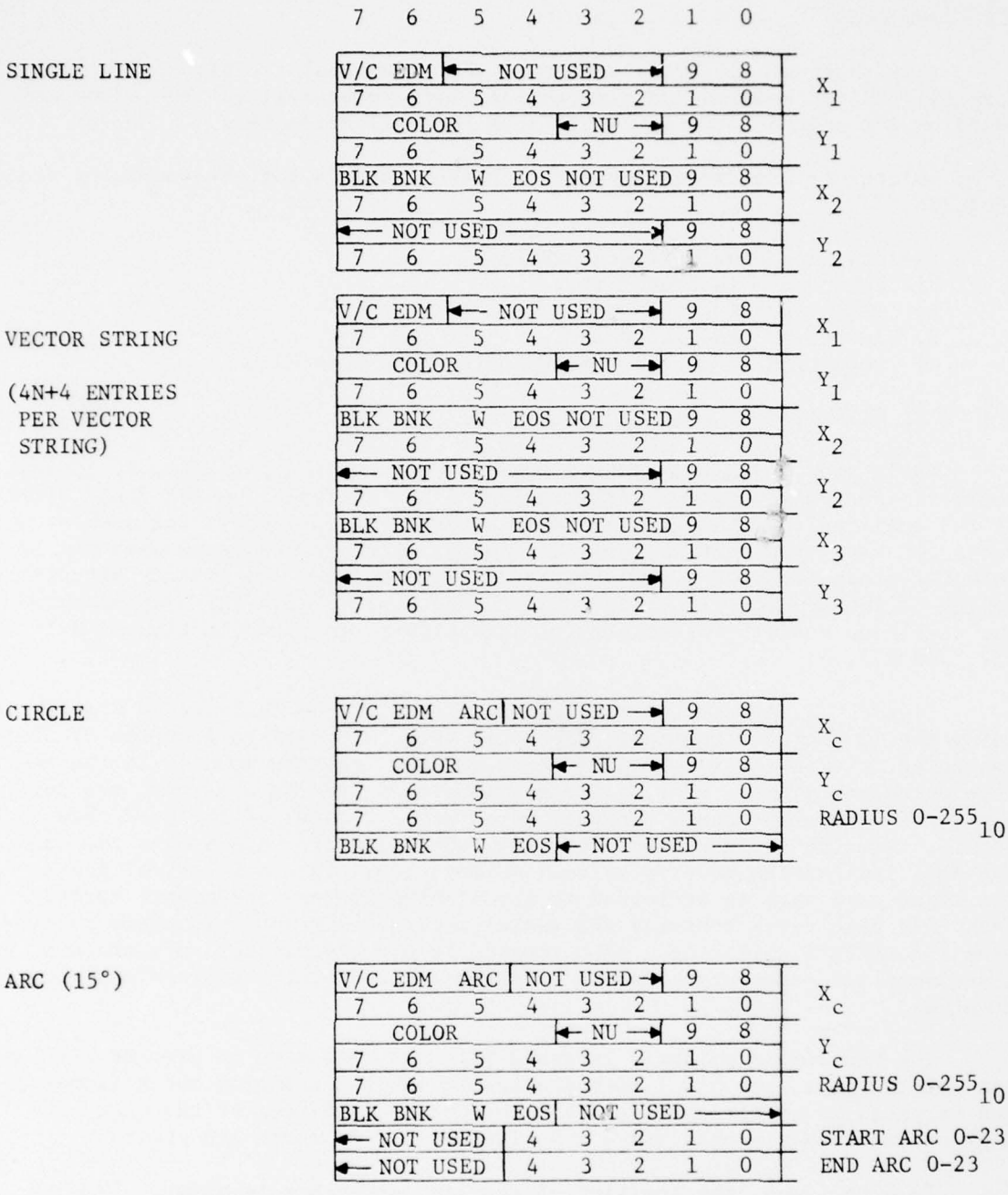


Figure 8-1. Vector Information as Stored in Microprocessor Unpainted Vector Table

9.0 PACKAGING

This phase of the study addressed the conceptual techniques of color terminal cabinet housing and electronics/hardware packaging. The study was based on the usage of the 13 and 15 inch 90° deflection CRTs.

Objectives identified to establish the criteria for the packaging study included:

a) dual and single screen displays,
b) enhanced maintainability,
c) minimized size,
d) increased modularity and,
e) reduction of manufacturing costs where possible.

9.1 DUAL DISPLAY

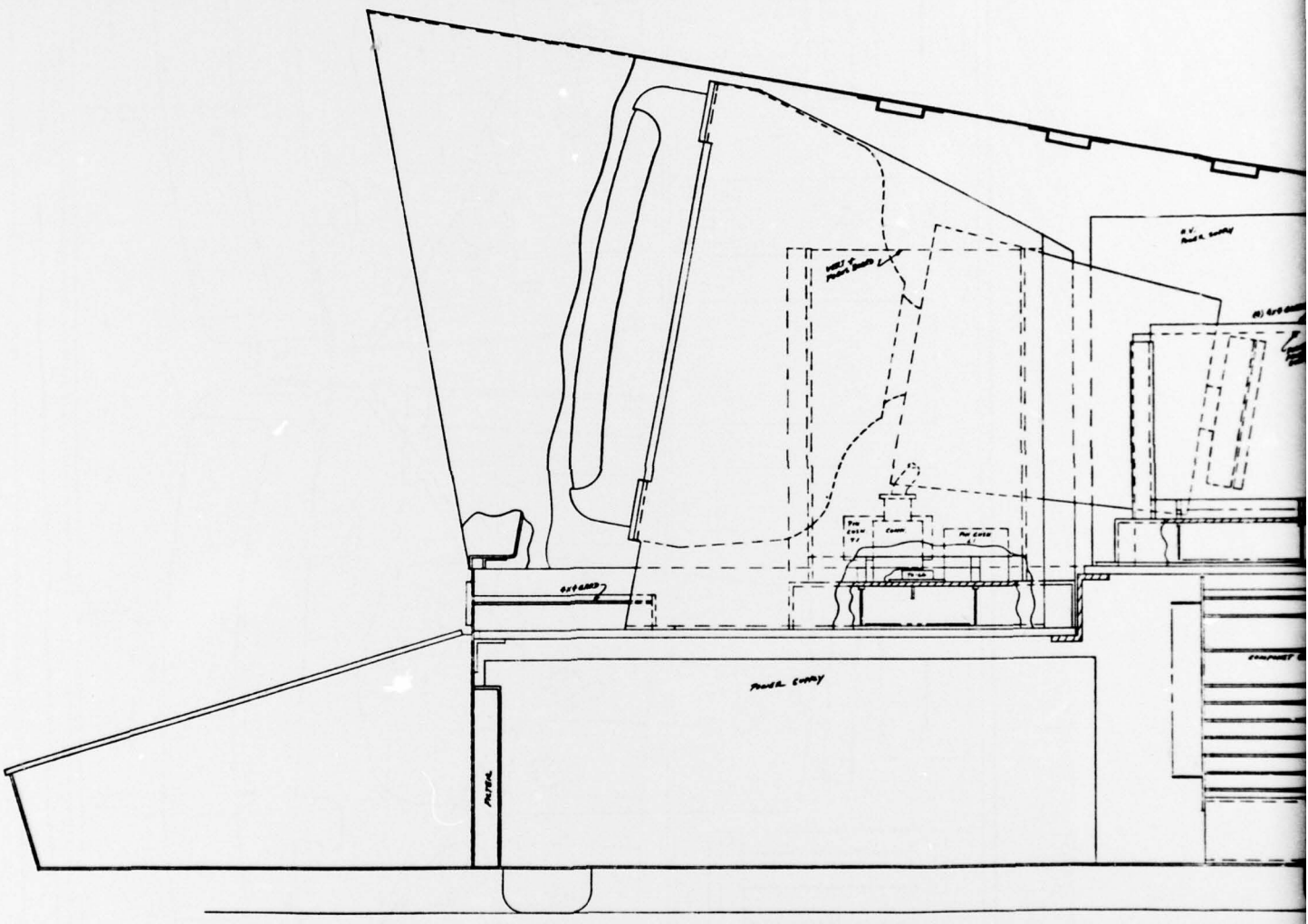
Early studies in the program were directed to the packaging of 15 inch monitors in a dual display configuration. This approach was abandoned after it was realized that the physical size would be objectionable for desk or table top use. Redirection for dual monitor displays was taken when the 13 inch CRT proved feasible from a technical standpoint. The modular circuit design of the monitor electronics and the decrease of the CRT size enhanced the packaging study. The results of this effort are shown in Figures 9.1, 9.2, and 9.3.

Figure 9.1 depicts the side and rear view of the dual screen display using the 13 inch CRT monitor. The logic circuitry differs from the OJ-389(V) packaging in that the triple wide cards are horizontally mounted in the rear base of the terminal. From the rear exposure, it can be seen that two card cages are accessed through the rear apron after removal of the card cage covers. Viewing the unit from the rear, the left card cage houses the controller, instruction memory, refresh memory, I/O, and other control logic. The right card cage is dedicated to the graphic control and memory cards. Each card cage cover contains RFI gasket material screwed into place to provide for TEMPEST shielding. Also located in the base of the unit are the power supplies necessary to power both the logic circuits and monitor electronics.

The monitor is slightly recessed into the base area to provide clearance between the tube, the 5 x 7 inch electronic cards containing the horizontal and vertical sweep circuits, and the shroud. To the rear of the unit, the high voltage power supply and 4 x 4 video amplifier cards are shown.

In both views, the position of the I/O connectors is shown. This approach allows the back panel and connector wiring to be completed as a subassembly before installation into the main base assembly.

Figure 9.2 shows the top view of the unit which makes up the monitor, its associated electronics, and the video amplifiers. Since each unit is assembled in the same manner, only one will be explained in this writing.


PANEL CARRY

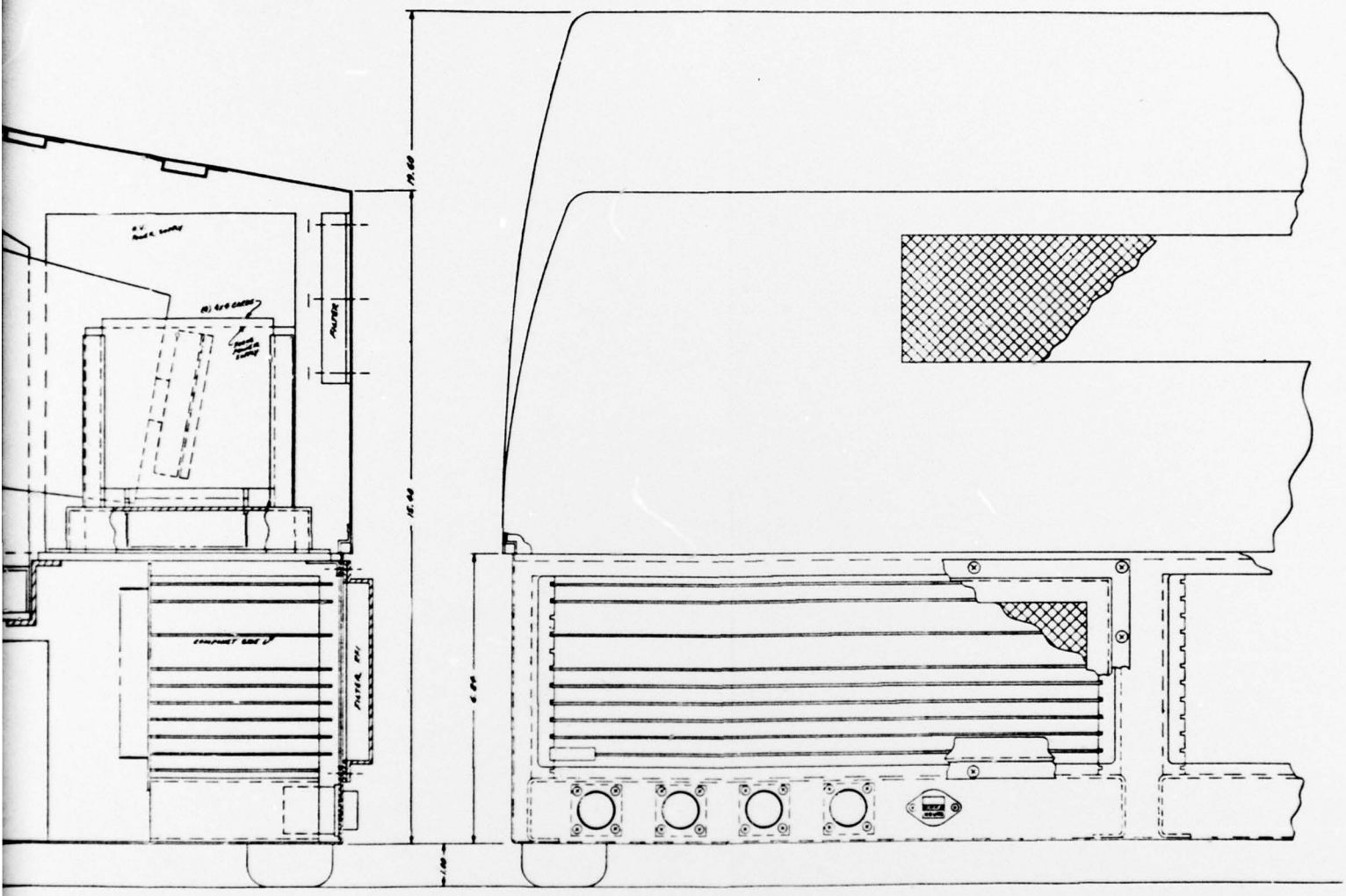


Figure 9.1 Dual Screen Configuration,
Side and Rear View

2

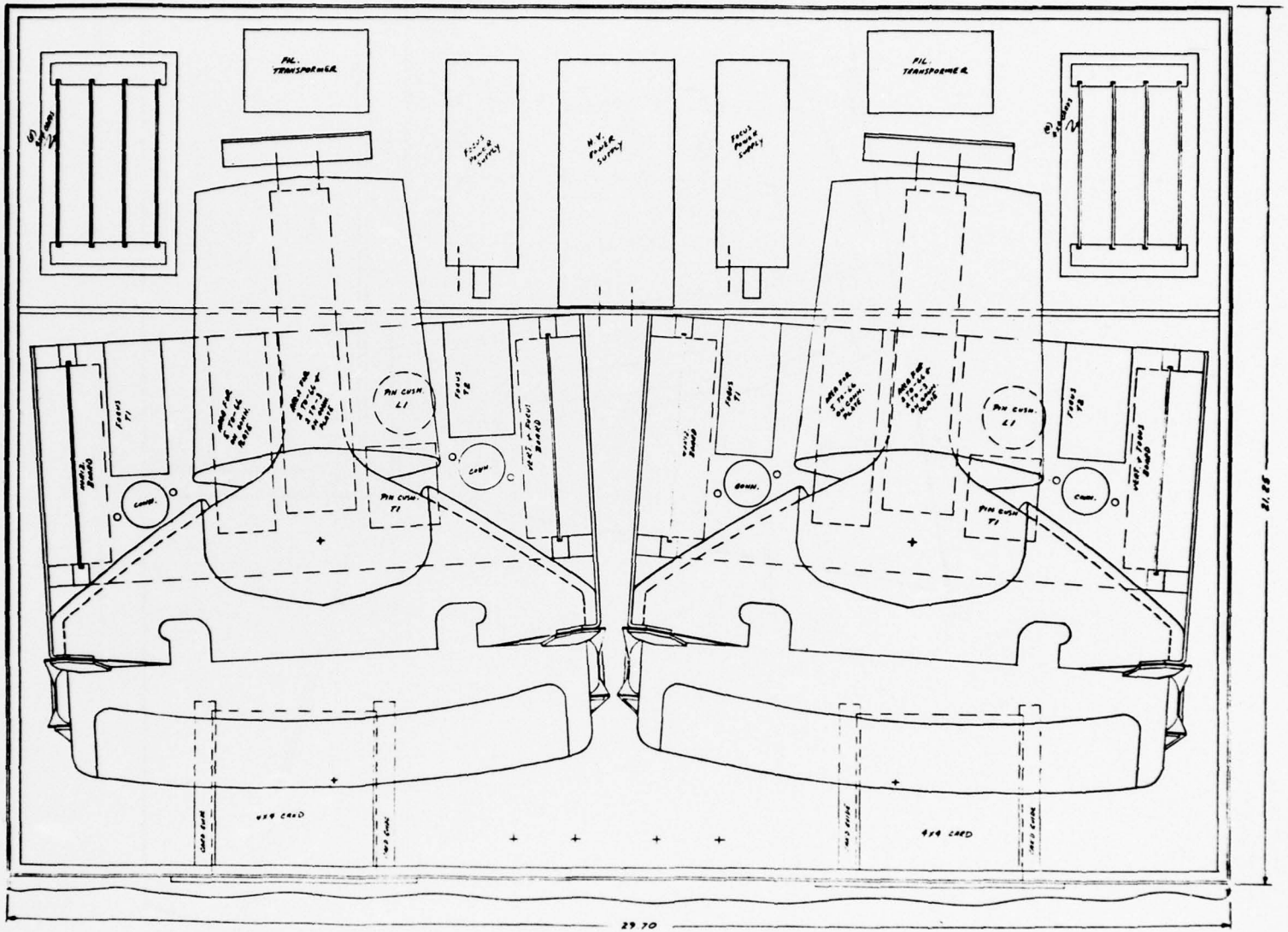


Figure 9.2 Dual Screen Configuration, Top View

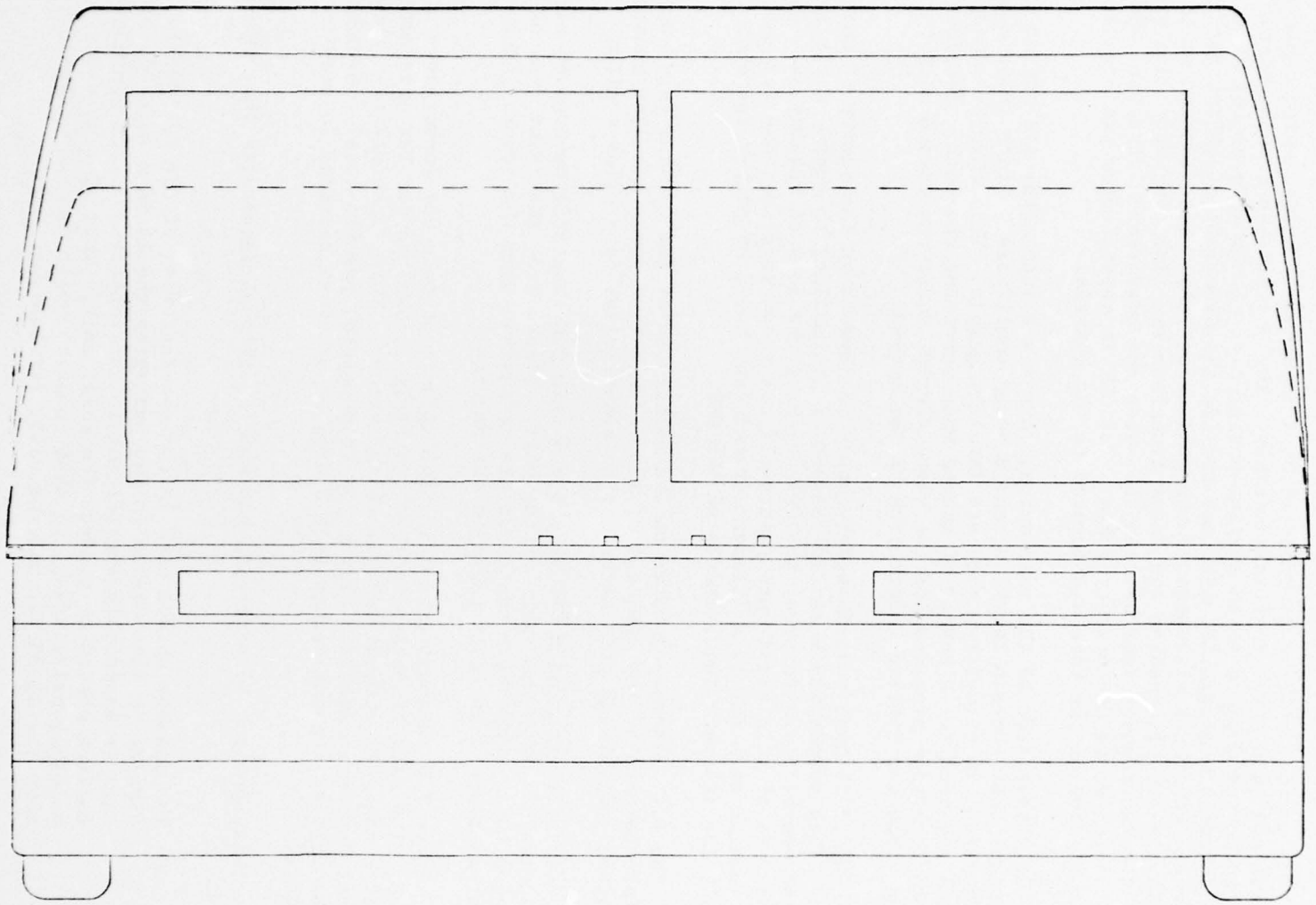


Figure 9.3 Dual Screen Configuration, Front View

Reference to Figure 9.1 will be required for this explanation.

The monitor will be constructed on a subassembly basis, which enhances checkout and test prior to final assembly. The chassis shown supports two 5 x 7 inch card mounted in an upright position on either side of the CRT. These boards are pluggable units and provide the necessary circuitry for horizontal and vertical sweeps to the deflection yoke. Also located on this chassis are the pin cushion and focus transformers. Two connectors are provided for interconnections between the sweep and convergence circuitry and the deflection and convergency yokes. The CRT is supported by two brackets on either side of the tube and mounted to the chassis.

On either side of the rear apron, four 4 x 4 inch cards are housed in card cages that contain the R, G, and B video amplifiers. Since these cards are identical in circuitry, they are interchangeable. This modular concept reduces the need for a number of spaces when servicing the unit. The fourth card in each cage provides for the video control functions needed when intermixing video and digital information on the screen.

The 25 KV high voltage power supply is located in the center of the rear apron. This supply was selected because of its ability to supply sufficient current capabilities to power two CRTs without the loss of regulation. On either side of this supply are separate focus power supplies, one for each CRT. Behind each CRT is a filament transformer rated at proper currents to satisfy the filament requirements of the CRT.

The P.C. assembly located on the socket end of the CRT not only supplies the interconnect to the elements of the CRT electron guns, but also houses the screen adjustment pots necessary to properly set up a color monitor.

Directly under each CRT is a 4 x 4 inch P.C. assembly mounted on slides and accessible from the front of the unit. Figure 9.3, the front view of the proposed unit, shows that the cards are accessible from the front. (They appear as slots under each table in the drawing.)

These P.C. assemblies contain the adjustment pots for convergence of the screen. The ease of access to these controls allows the service personnel to converge each CRT without removal of the shroud. This, combined with the new circuit approach explained earlier in this report, permits total convergence of the unit in minutes rather than hours, as has been required in previous monitors.

This approach to packaging has some additional advantages that should be noted:

a) The present shroud used in the manufacturing of the OJ-389(V) display is also usable in the packaging the 13 inch color display. This is especially significant in the reduction of the nonrecurring dollars needed to produce the color unit. This also provides for a possible price break, in that quantity units may be purchased for both the OJ-389(V) and the color terminal.

b) The keyboard height remains the same and, with the exception of the additional color cluster switches required for color displays, is applicable to both the OJ-389(V) and color.

One primary difference in overall appearance between the monochrome and color dual screen displays is that the base is raised approximately to 1 1/2 inches between the keyboard and shroud in the color dual screen display. This was necessary primarily to gain the extra height required for the CRT, provide convergence circuitry accessibility, and gain sufficient height to house the logic circuitry in the rear of the base. As a result, new tooling would be required for the base of the unit.

9.2 SINGLE DISPLAY

Figures 9.4, 9.5, 9.6, and 9.7 depict the proposed single display configuration. In these figures, the 15 inch CRT is packaged in a manner identical to that explained for the 13 inch dual display. Therefore, only changes in packaging concepts will be pointed out in this text.

Figures 9.4 and 9.5 show the location of the triple wide logic P.C. assemblies. Because of the narrowness of the unit, only one card cage is located in the base area. These cards represent the controller electronics. The optional graphics circuitry is located on the top apron of the unit, to the right of the CRT.

Figure 9.6 shows the rear of the unit with the I/O connectors located to the left of the controller card cage cover. Access to convergence circuit adjustments are again located under the CRT, as shown in Figure 9.7. The keyboard for this unit has not been detailed because of various options and user requirements that would affect the functional layout.

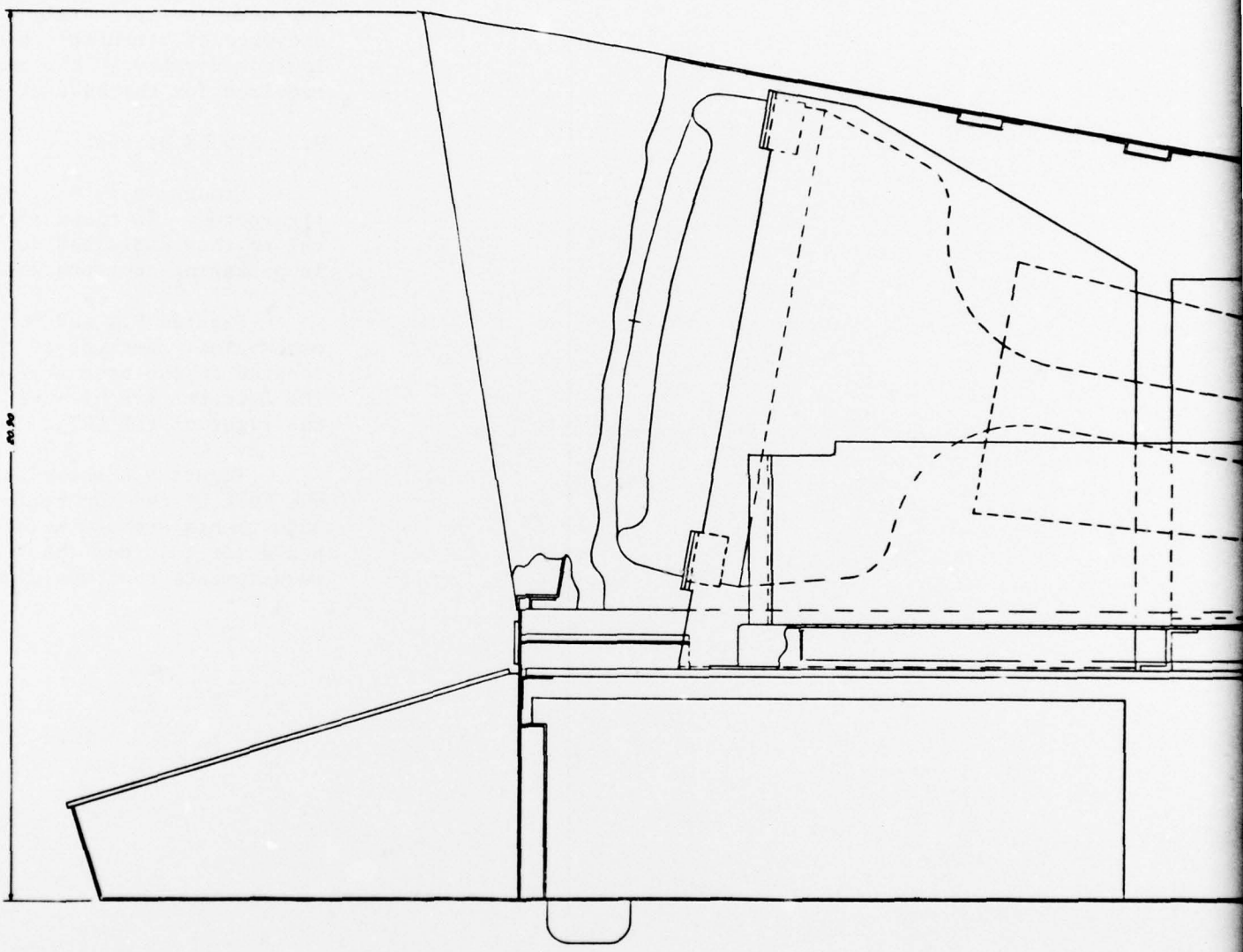


Figure 9.4 Si

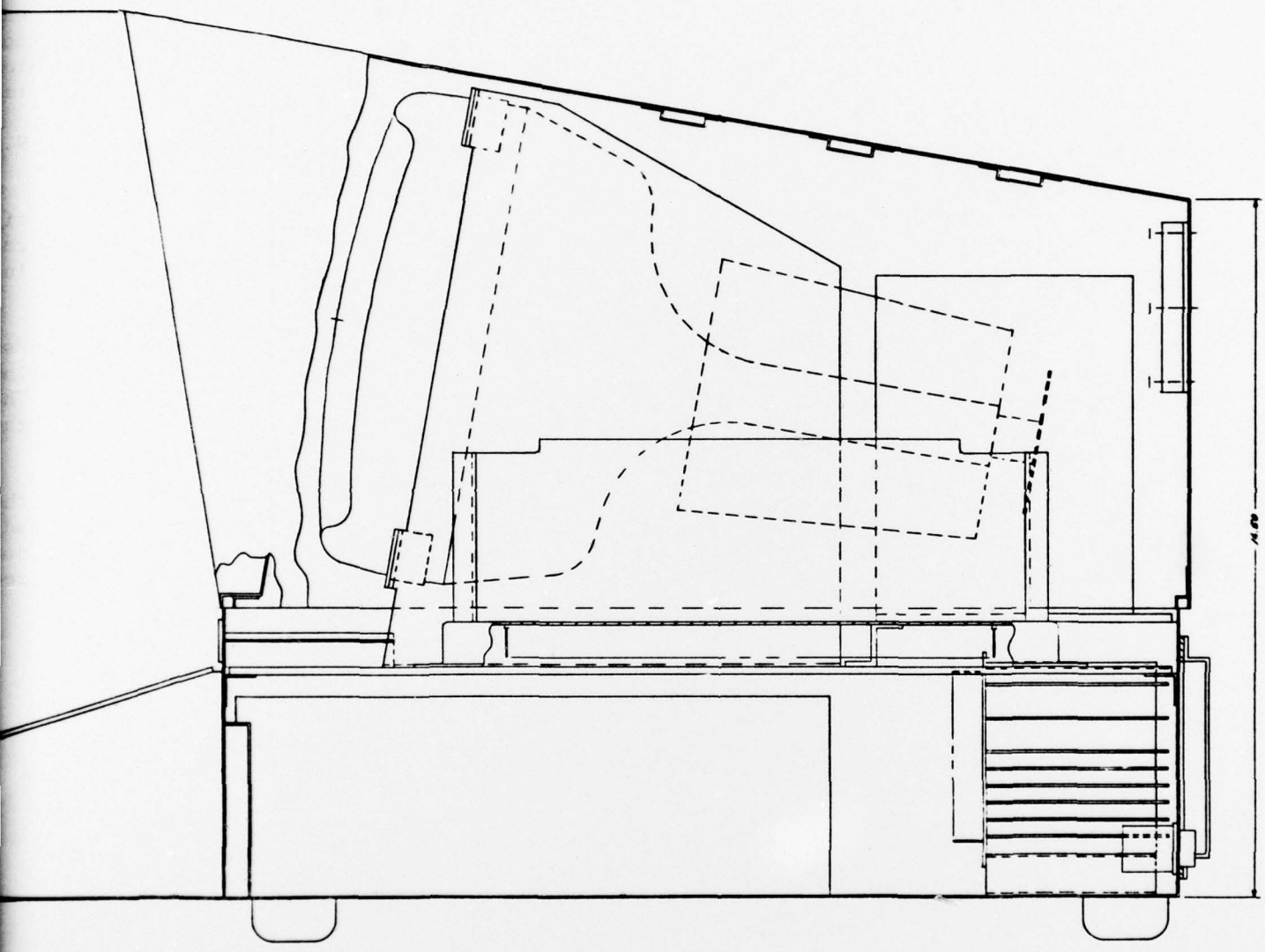


Figure 9.4 Single Screen Configuration, Side View

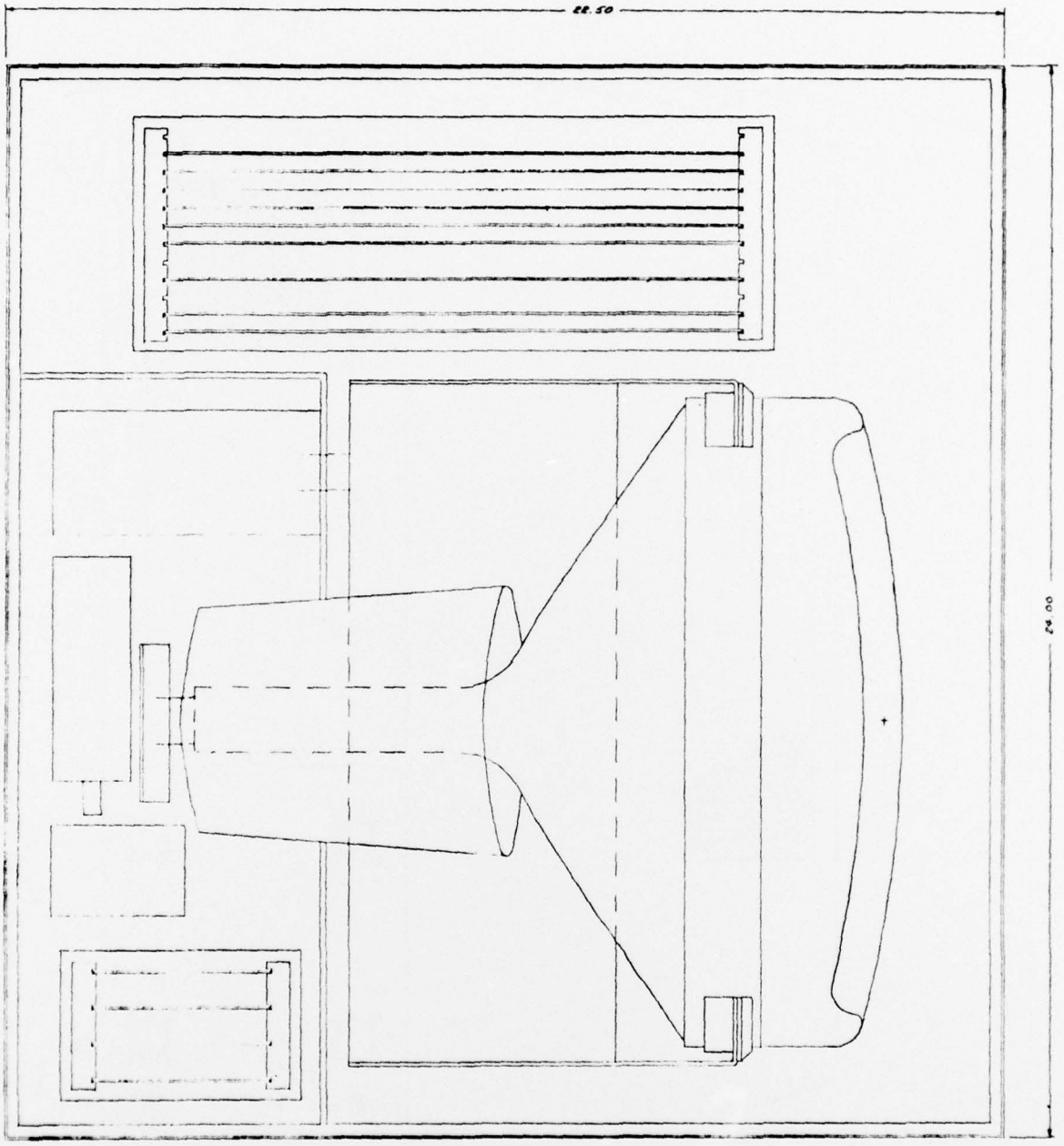


Figure 9.5 Single Screen Configuration, Top View

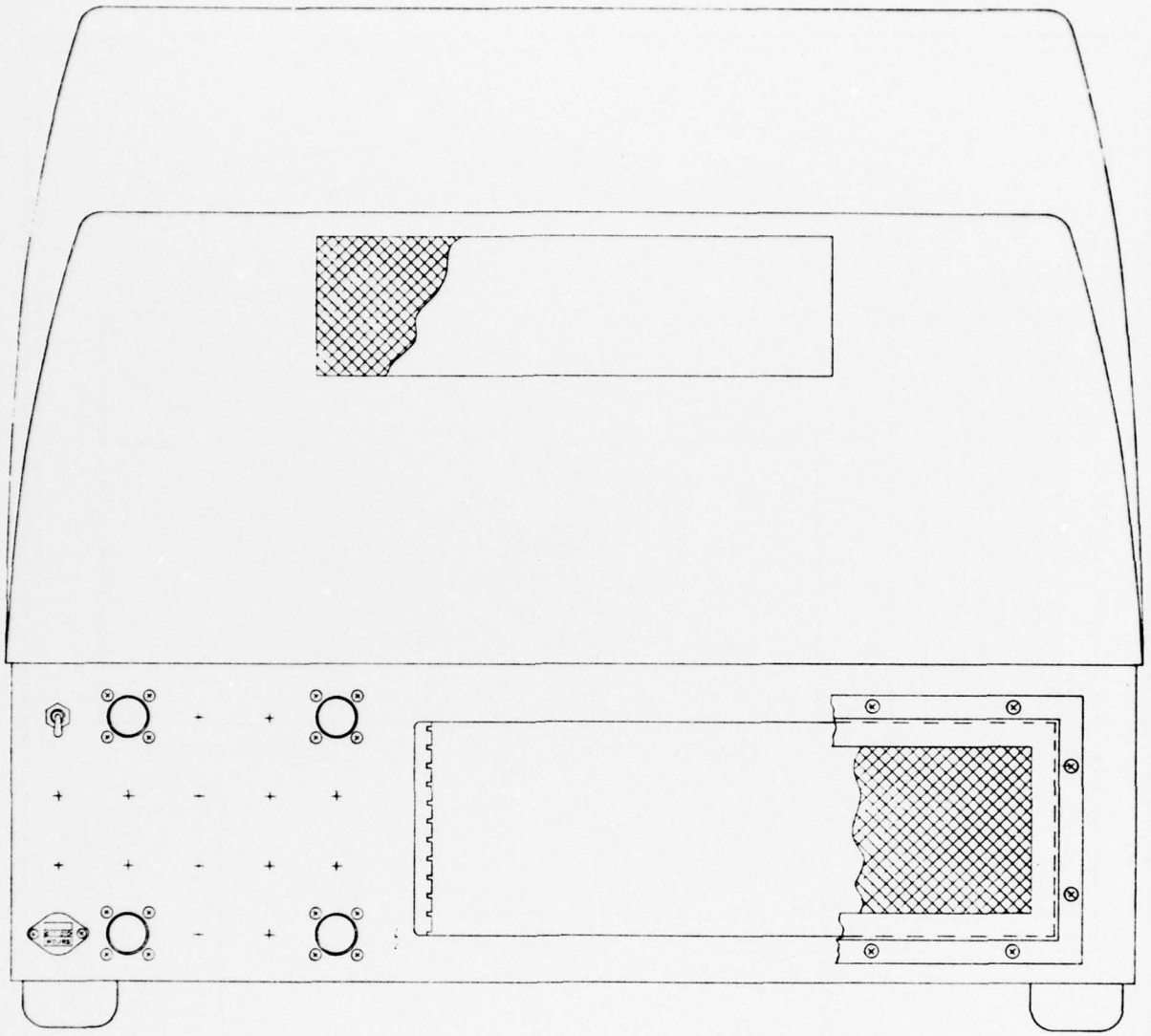


Figure 9.6 Single Screen Configuration, Rear View

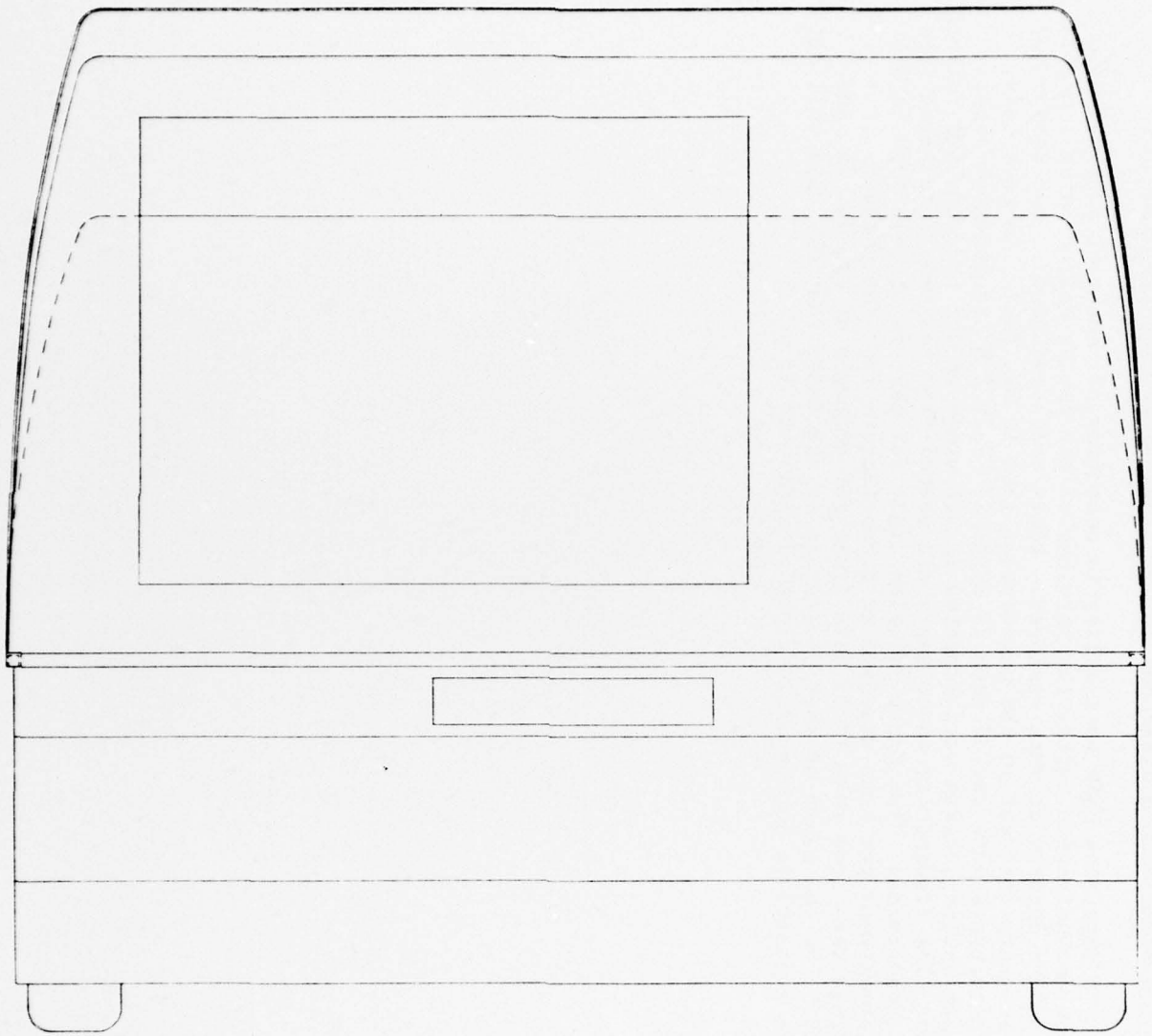


Figure 9.7 Single Screen Configuration, Front View

10.0 SAFETY

A considerable amount of concern has been expressed for the safety of operating personnel in close contact with a terminal display where anode voltages are in the 20 to 28 KV range. This concern is primarily that X-ray emission might become hazardous to personnel after extended exposure.

To determine this possibility in operating of the color monitors used in the demonstration units, the services of the Sperry Univac Safety, Medical, and Health department were employed. Tests were conducted on two unshrouded sample units resident in the engineering labs in St. Paul. In each case, anode voltages were varied from 22 KV to 28 KV in 2 KV incremental steps. At each setting, tests were repeated in all areas of the CRT and high voltage areas. The findings of these tests are quoted from the report received from this department: "The X-ray emission limit for devices of this type is 0.5 milliroentgens per hour measured at 5 centimeters from the surface. All readings were less than 1% of this limit for voltages of 22, 24, 26, and 28 KV." On the basis of these tests, it is concluded that the unit will not cause a hazard to personnel in close proximity to it.

11.0 CONCLUSION

As depicted in the text of this report, all objectives of the study identified by the statement of work have been met and completed. Technical breakthroughs have been made on circuitry heretofore considered technical risks. A typical example of this is the new approach to convergence in color monitors.

In the presentation of the study, results and the demonstration of the "breadboard" model held on 15 April 1977 at the Sperry Univac facility in St. Paul, Minnesota, it was shown that the use of color in the next generation of display terminals is not only feasible but will become necessary and in some instances critical for operator perception and efficiency of the more complex screens being presented from an ever-increasing data bank.

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